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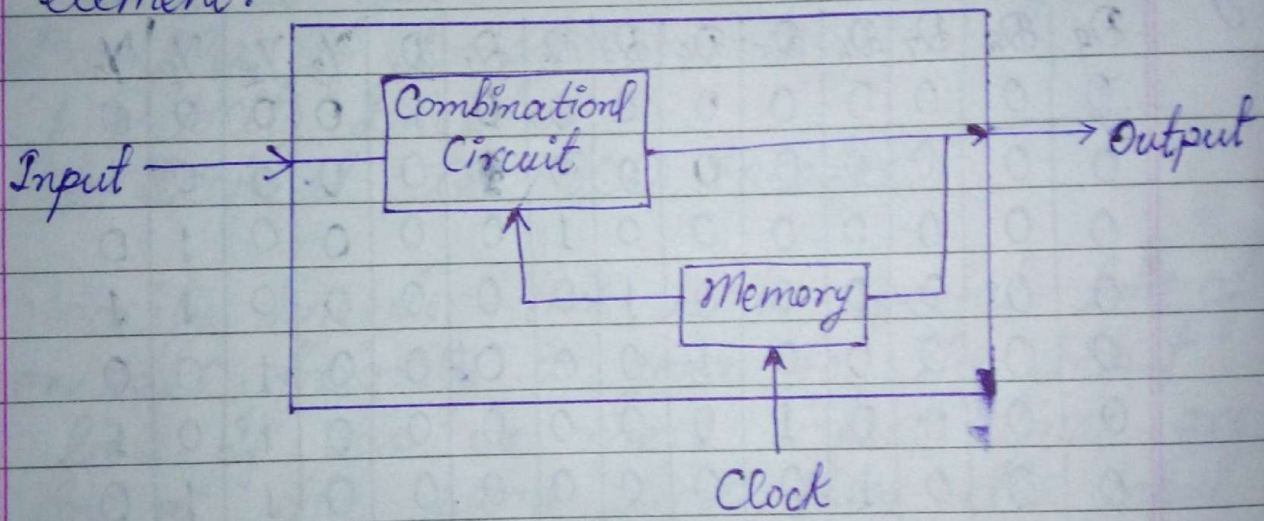
II Unit

Sequential Circuit-

The combinational circuit does not use any memory hence the previous state of input does not have any effect on the present state of the circuit but sequential circuit has memory so output can vary based on input. This type of circuit uses previous input output clock and memory element.



Flip-Flop-

This is a sequential circuit which generally samples its inputs and changes its output. Only at particular instance of time and not continuously flip-flop is said to be edge sensitive or edge trigger rather than being level triggered like latches.

Trigger -

A trigger is a small device that release a spring or catch and so sets of a mechanism specially in order to fire a gun

Latches -

A latch is an example of a vice table multiviberator that is a device exactly the two stable state.

These states are equals to high or low (O/P).

SR Circuit (Set-Reset) -

It is basically SR latches using NAND Gate with an addifional enable input. It is also called as level triggered SR flip-flop. For this circuit output will take place if and only if the enable input E is made active. In short, this circuit will operate as an SR Latch. if E=1 but there is no change in output if E=0.

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A RS flip-flop is the simplest possible element. It is constructed by feeding down outputs of two NOR Gates or NAND Gates.

The inputs R and S are referred to as the reset and set input respectively.

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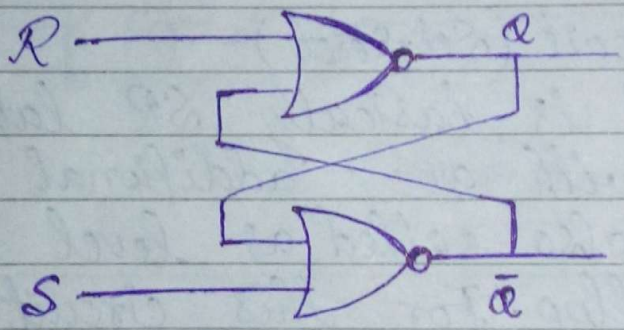
To understand the operation of RS flip-flop consider the following scenario.

NOR:-

R	S	Output		Comment
		Q	$\bar{Q}$	
0	0	Q	$\bar{Q}$	Hold State
0	1	1	0	Set state
1	0	0	1	Reset State
1	1	?	?	Unknown or avoidable condition



NAND:-

R	S	Output		Comment
		Q	$\bar{Q}$	
0	0	?	?	Unknown condition.
0	1	0	1	Reset
1	0	1	0	Set
1	1	Q	$\bar{Q}$	Hold State

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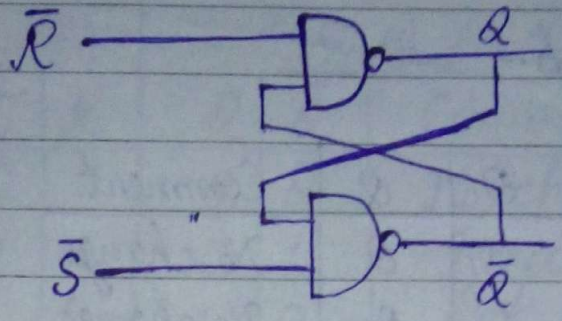
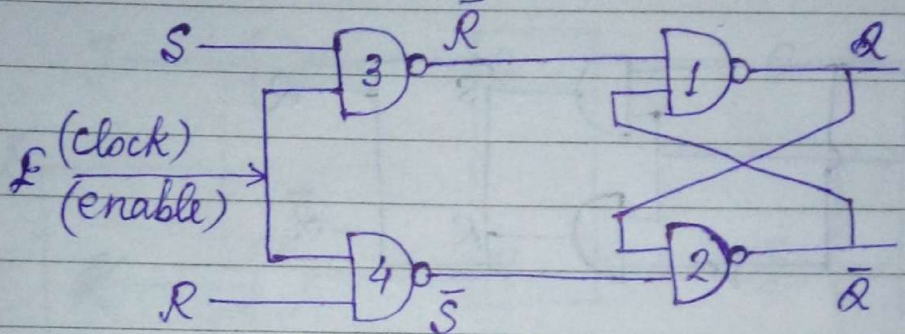


Clock SR flip-flop-



* Set on → output/set (Q), Reset on → output/reset ($\bar{Q}$).
when E=0 then on that it work as simple SR flip-flop or unclock SR flip-flop.

E	S	R	Q	$\bar{Q}$	Comment
1	0	0	Q	$\bar{Q}$	Hold
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	?	?	Unknown/Avoid condition

when enable condition is 1 then it work as R-S NOR Gate.

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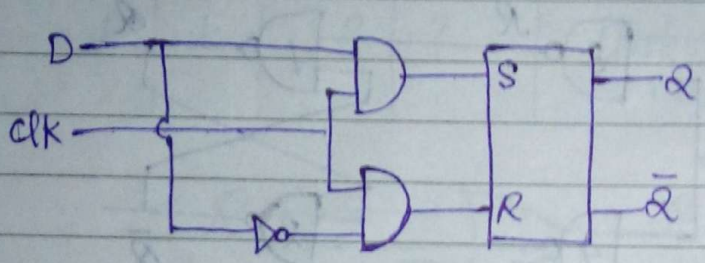
D - Flip-Flop -

Clock	D	Q	Comment
0	0	Q	No change
0	1	Q	No change
1	0	0	No value
1	1	1	Value



Master Slave JK Flip-Flop -

Master Slave JK flip-flop is a cascode of two S-R flip-flop with feedback from the output of second two input of first.

Master is a positive level (1) trigger but due to the presence of inverter in the clock line the slave will respond to the negative level (0) Hence when the clock = 1 i.e., positive level on this level master is active and the slave is inactive clock = 0 then slave is active and master is inactive.

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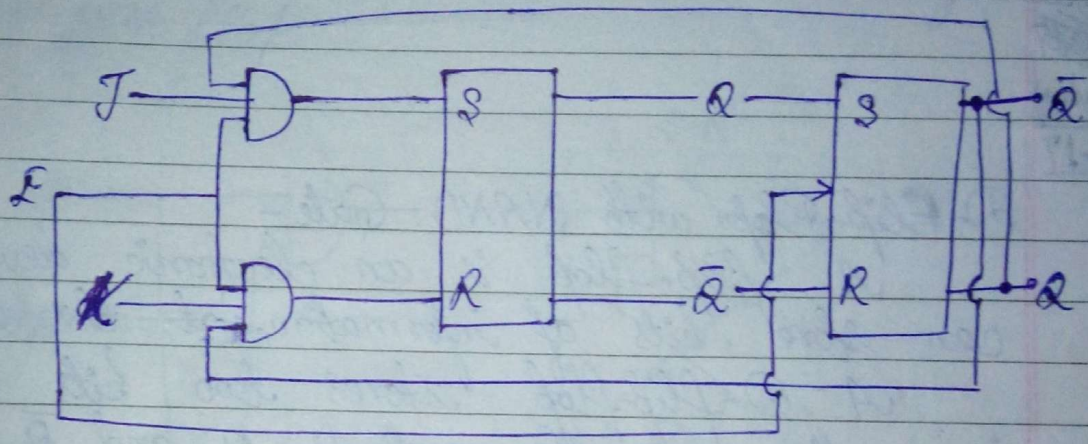
Input			Output		
Clock (C)	J	K	Q	$\bar{Q}$	Comment
1	0	0	Q	$\bar{Q}$	No change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	$\bar{Q}$	Q	Toggle.



Operations—

(i) When J=K=0 (No change)
When clock=0 the slave = active and master equals to inactive but since the S & R input are not change the slave output will also remain unchanged therefore output will not change if J=K=0.

(ii) J=0 and K=1 (Reset condition)
When clock=1 the master = active and slave equals to inactive therefore output of the master become Q=0 and $\bar{Q}$=1 that means $\bar{Q}$=0 and Q=1.

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When clock=0 on that time slave = active and master = inactive therefore output of the slave become $Q=0$ and $\bar{Q}=1$, again clock=1 that time master is active, slave = inactive even with the changed output $Q=0$ and $\bar{Q}=1$ feedback to the master so that again $\bar{Q}=0$ and $Q=1$.

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D-Flip-Flop with NAND Gate -

A flip-flop is an electronic device that can store bits of information. ~~at the outputs~~

A D-flip-flop stores two bits of information at the outputs Q and $\bar{Q}$.

Q and $\bar{Q}$ are always opposite for each other in terms of logic states. Thus, if $Q=1$ and $\bar{Q}=0$.

The D-flip-flop has a single input.

lowest level = 0 and highest level = 1.

The D-type flip-flop are constructed from a gated SR flip-flop with an inverter added between the S and R input to allow for a single input.

This single input is called the data input.

If this data input high, flip-flop will ~~would~~ be set and when the data input is low then flip-flop will be reset.

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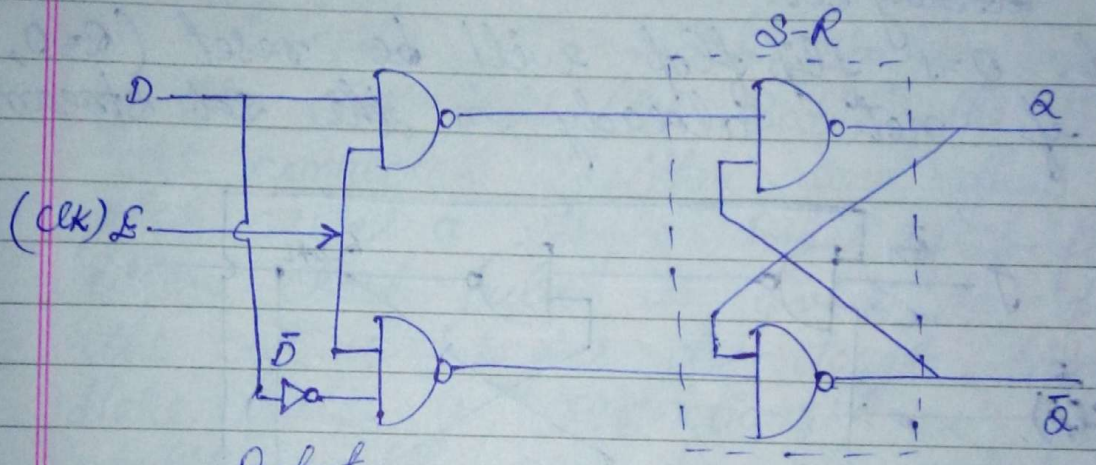
To avoid an additional input called the "clock" or "enable" is used to isolate the data input from the flip-flop latching. This form happening an inverter can be connected between the set and reset input to produce another type of circuit known as data latch or delay flip-flop.



Input

(E) clk	D	Q	$\bar{Q}$	Comments
0	X	Q	$\bar{Q}$	Memory no change
1	0	0	1	Reset
1	1	1	0	Set

Basic J-K flip-flop (Simple):-

Both the S and R inputs of the previous S-R ~~flip~~ bistable have now been replaced by two inputs called the J and K inputs.

Here J=S and K=R.

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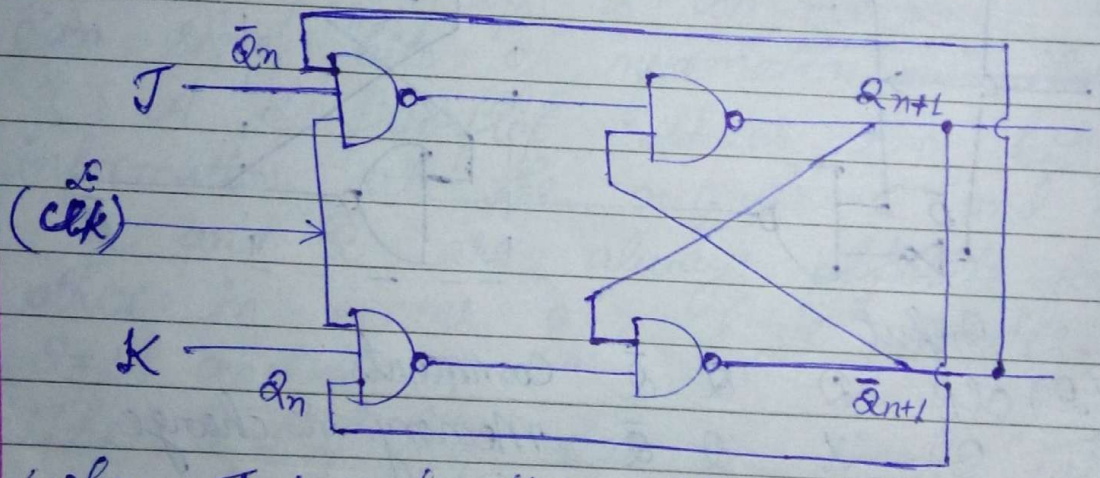
These J and K inputs disable the NAND gates therefore clock pulse have no effect on the flip flop.
In other words Q return its last value.
When J=0 and K=1 the upper NAND gate is disabled the lower NAND gate is enable.
~~If Q=1 flop flop this is set.~~
~~If $\bar{Q}$=1 the result will be set. and if not already set.~~
If Q=1 flip flop will be reset (Q=0, $\bar{Q}$=1) if not already in the set stream.



When J=1 and K=0 the lower NAND Gate is disabled, the upper NAND Gate is enabled.
If $\bar{Q}$=1 flip flop will be set (Q=1, $\bar{Q}$=0) if not already in the reset stream.

When J=1 and K=1, if Q=0, the lower NAND Gate is disabled and upper NAND Gate is enabled, so Q_{n+1}=1.
On the other hand if Q=1 the lower NAND Gate is enabled on that time

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$Q_{n+1} = 0$ and $\bar{Q}_{n+1} = 1$

Clk	J	K	Q_{n+1}	$\bar{Q}_{n+1}$	Comment
1	0	0	Q_n	$\bar{Q}_n$	No change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	$\bar{Q}_n$	Q_n	Toggle

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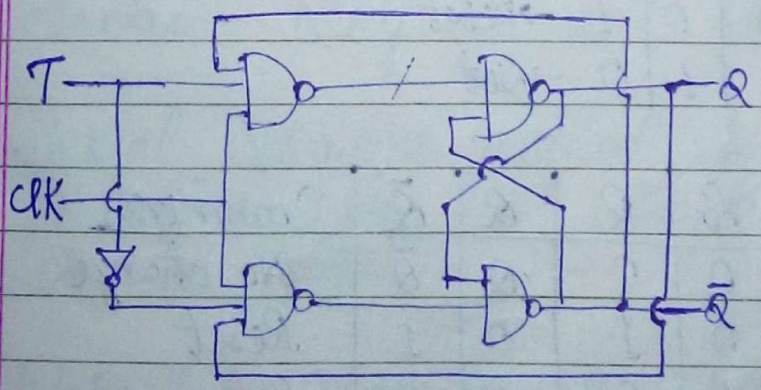
T- Flip-Flop:-

This is a much simpler version of the J-K flip-flip. Both the J and K are connected together and thus are also called a Single Input flip-flop. When clock pulse is given to flip-flop the output begins to toggle (triggered). Here also a restrictions on the pulse width can be eliminated with a master slave or edge triggered construction.



Clk	Q_n	T	Q_{n+1}
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

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Proper O/P → sync
Improper O/P → async

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Edge Triggered

An edge triggered flip-flop changes states either at the positive edge or rising edge or at the negative edge or falling edge of the clock pulse on the ~~clock~~ control input. The three basic types are S-R, J-K and D.

The S-R, J-K and D inputs are called synchronous input because data on these inputs are transferred to the flip-flop output only at the triggering edge of clock pulse. On the other hand, the set and clear inputs are called asynchronous as they are inputs that effect the state of the flip-flop independent of the clock.

Example –

Input

~~Clk S R~~

eg. of D →

Clk	D	Q	$\bar{Q}$	
↑	0	0	1	→ Reset
↑	1	1	0	→ Set

Clk	S	R	Q	$\bar{Q}$	Comments
↑	0	0	Q	$\bar{Q}$	No change
↑	0	1	0	1	Reset
↑	1	0	1	0	Set
↑	1	1	?	?	Invalid

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(Simple) Registers-

A register is a group of flip-flop suitable for storing binary information. Each flip-flop is a binary cell capable of storing one bit information like n-bit register has a group of n-flip-flop.

The register is a type of sequential circuit and an important building block used in digital systems like multipliers, dividers, memories and microprocessors.

Shift Registers-

A register that is used to store binary information is known as a memory register. A register capable of shifting binary information either to the right or to the left is called shift register. There are two methods of shifting the data i.e. Serial Shifting and Parallel Shifting.

1.) Serial Shifting method shifts one bit at a time for each clock pulse in a serial fashion.

2.) Parallel Shifting - In parallel shifting operation, all the data get shifted simultaneously during a single clock pulse. So parallel shifting method.

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~~Doing~~ is much faster than the serial shifting method.

Shift Registers are classified into the following four types:

(i) SISO (Serial IN Serial OUT)
(ii) SIPO (Serial IN Parallel OUT)
(iii) PISO (Parallel IN Serial OUT)
(iv) PIPO (Parallel IN Parallel OUT)

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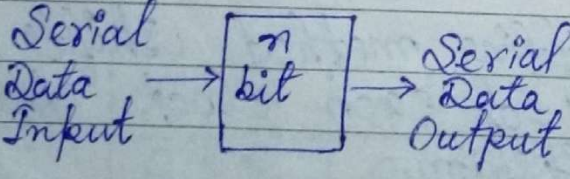
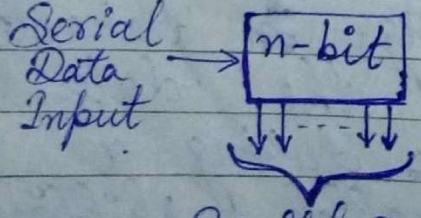
Shift registers are used in digital systems for temperory storage of information data manipulation and transferring.

In addition, they are used in counting circuits, such as simple counters, variable modulo counters, up/Down counters and increment counters.

(i) Serial In Serial Out-



(ii) Serial In Parallel Out-



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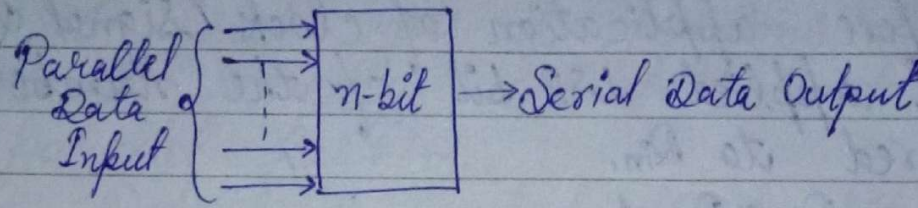
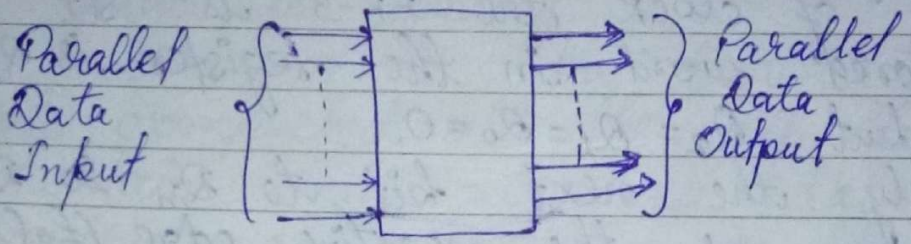
(iii) Parallel In Serial Out



(iv) Parallel In Parallel Out



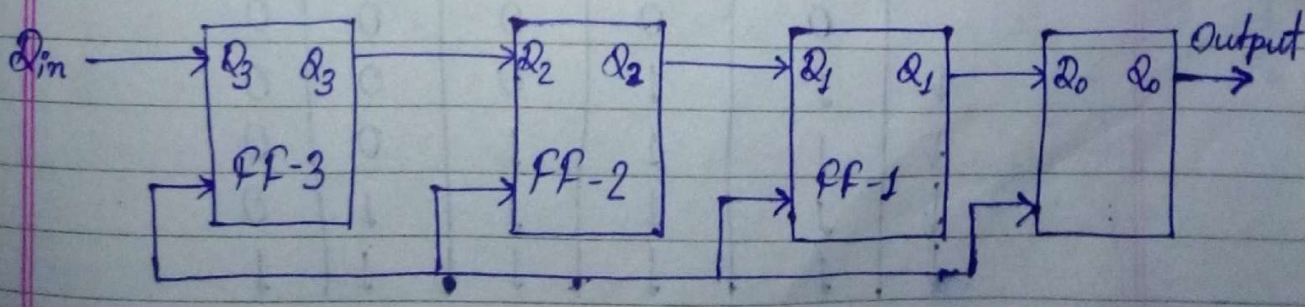
(i) SISO-

All the flip-flop be initially in the reset condition. i.e., $Q_3 = Q_2 = Q_1 = Q_0 = 0$

If any entry of four bit binary no. 1111 is made into the register. this no. should be applied to D_{in} bit with the ~~applied first~~ LSB (Load Shift Bit) bit applied first.

The D_{in} of FF-3 i.e., Q_3 is connected to Serial data input i.e., D_{in}

Output of FF-3 i.e., Q_3 is connected to the input of the next flip-flop i.e., Q_2 or so on.



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Operations-

(1.) Before application of clock signal $Q_3=Q_2=Q_1=Q_0=$ and applied LSB bit of the number to be entered to Q_{in}.

So $Q_{in}=Q_3=1$.

Apply the clock on the first falling edge of clock the FF-3 is set and stored word in the register is $Q_3=1$.

but $Q_2=Q_1=Q_0=0$.

(2.) Apply the next bit to Q_{in} so $Q_{in}=1$ as soon as the negative edge (falling edge) of the clock hits FF-2 will set and the stored word change to $Q_3=Q_2=1,1$ and $Q_1=Q_0=0,0$.

(3.) Apply the next bit to be stored i.e., $Q_{in}=1$ as soon as the third clock edge hits FF-1 will be set and the stored output will be modified to $Q_3\ Q_2\ Q_1\ Q_0 = 1\ 1\ 1\ 0$.

(4.) Similarly with $Q_{in}=1$ and with the fourth negative clock edge arrive in the stored word in the register is

$Q_3\ Q_2\ Q_1\ Q_0 = 1\ 1\ 1\ 1$

CLK	$Q_3=Q_3$	$Q_3=D_2$	$Q_2=D_1$	$Q_1=D_0$	Q_0
.	0	0	0	0	0
↓	1	1	0	0	0
↓	1	1	1	0	0
↓	1	1	1	1	0
↓	1	1	1	1	1

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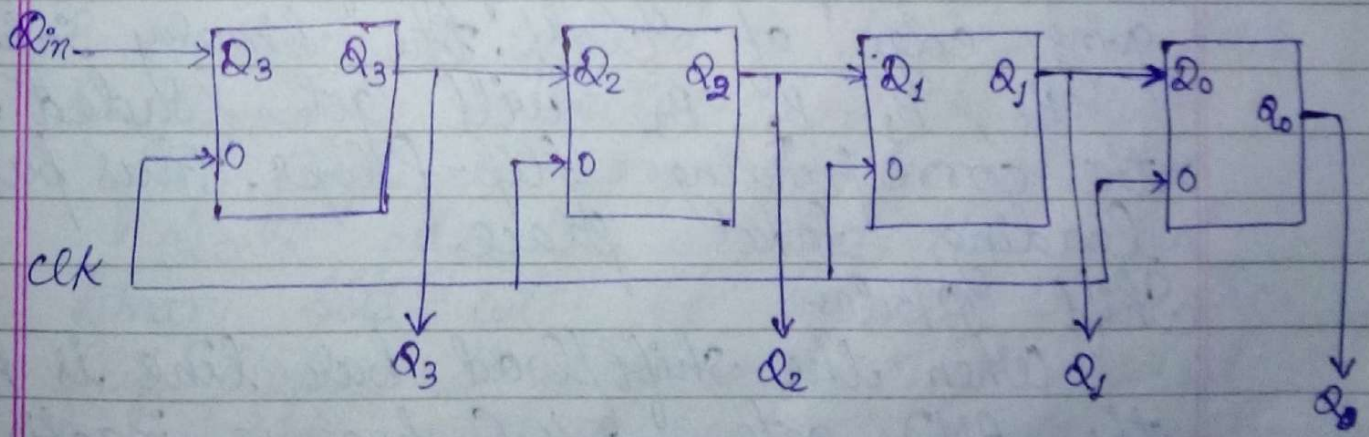
Serial Input Parallel Output :-

In such types of operations the data is entered serially and taken out in parallel fashion.

Data is loaded bit by bit. The outputs are disabled as long as the data is loading.

As soon as the data loading gets completed all the flip flops contain their required data, the outputs are enabled so that all the loaded data is made ~~overall~~ available overall the output lines at the same time.

4-clock cycles are required to load a four bit word. Hence the speed of operation of SIPO mode is same as that of SISO mode.



Parallel Input Serial Output-

Data bits are entered in parallel fashion.

The circuit shown below is a four bit parallel input serial output register.

Output of previous flip-flop is connected to the input of the next one via a combinational circuit.

The binary input word B_0, B_1, B_2, B_3 is applied through the same combinational circuit.

There are two modes in which this circuit can work namely - shift mode and load mode.

Load Mode-

When the shift/load bar line is low (0), the AND gate 2, 4 and 6 become active, they will pass B_1, B_2, B_3 bits to the corresponding flip-flops. On the low going edge of clock, the binary input B_0, B_1, B_2, B_3 will get loaded into the corresponding flip-flops. Thus parallel loading takes place.

Shift Mode-

When the shift/load bar line is high (1), the AND gate 2, 4, 6 become inactive. Hence the parallel loading of the data becomes impossible. But the AND gate 1, 3 and 5 become active. Therefore,

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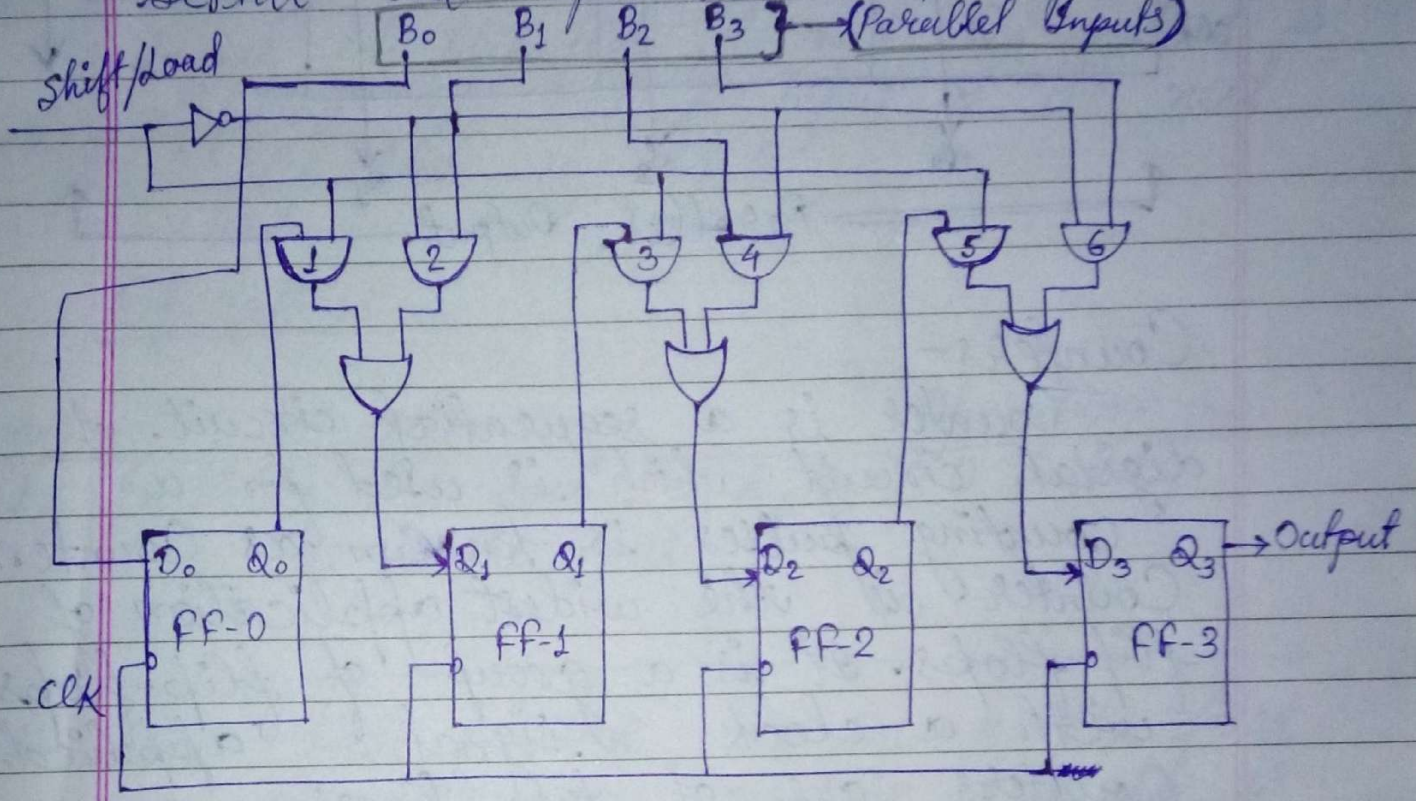
the shifting of data from left to right bit by bit on application of clock pulses. Thus the parallel in serial out operations takes place.



PIPO (Parallel In Parallel Out)–

In this mode, the 4-bit binary input B_0, B_1, B_2, B_3 is applied to the data inputs D_0, D_1, D_2, D_3 respectively of the four flip-flops. As soon as a negative clock edge is applied, the input binary bits will be loaded into the flip-flops simultaneously. The loaded bits will appear simultaneously to the output side.

Only clock pulse is essential to load all the bits.

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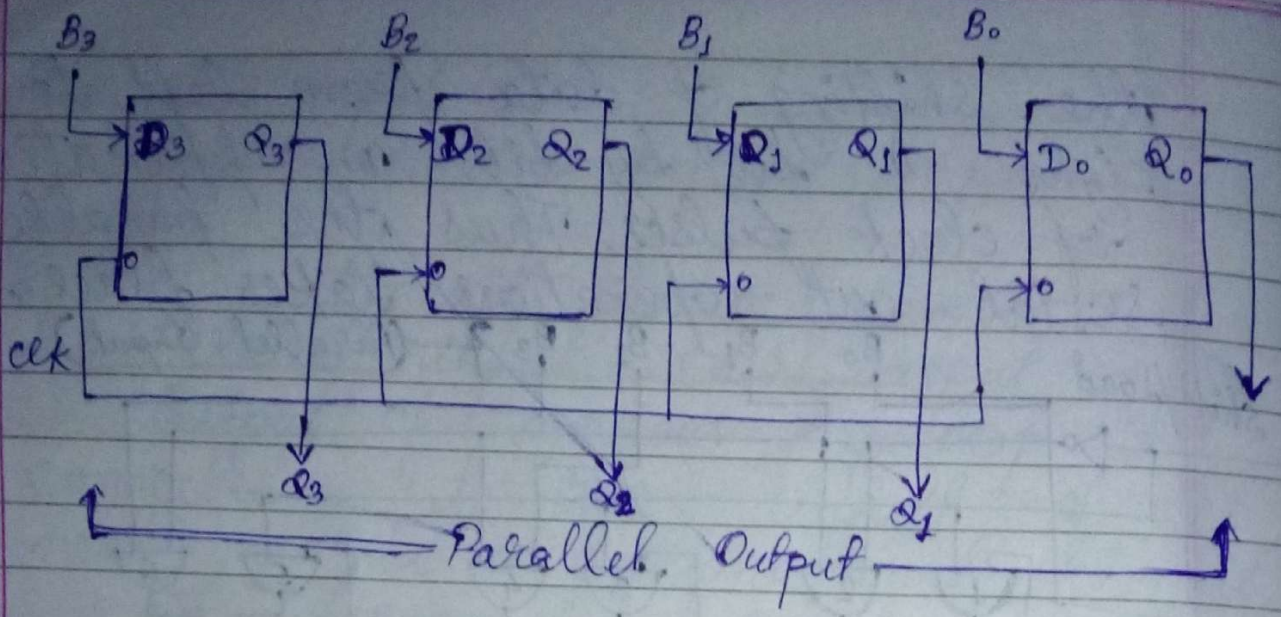
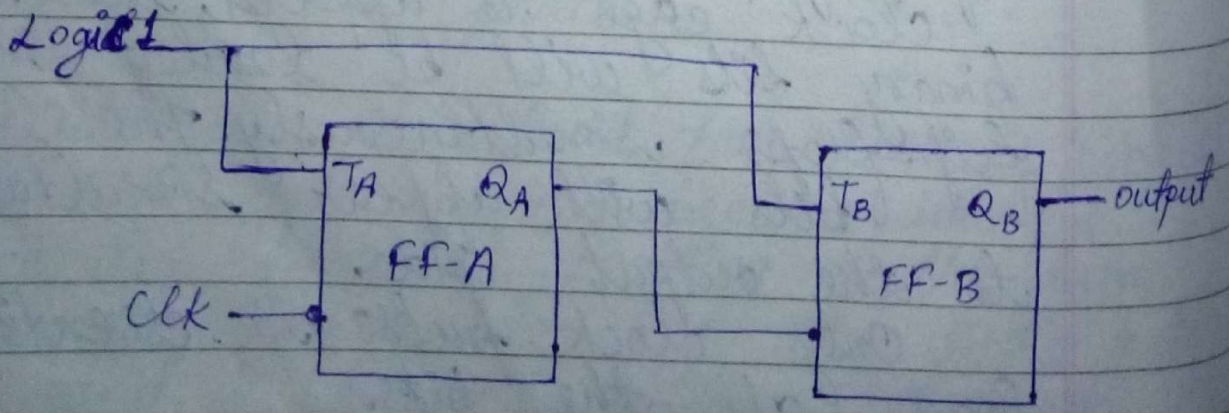


Counters–

Counter is a sequential circuit. A digital circuit which is used for a counting pulses is known as Counter. Counter is the widest application of flip-flops. It is a group of flip-flops with a clock signal applied. Counters are of two types.

(i) Asynchronous or Ripple Counters
(ii) Synchronous Counters.

(i) Asynchronous or Ripple Counters:- The logic diagram of a 2-bit ripple up counter is:



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The toggle (T) flip-flop are being used. But we can use the J-K flip-flop also with J and K connected permanently to logic 1. External clock is applied to the clock input of flip-flop A and Q_A output is applied to clock input of the next flip-flop i.e. FF-B

Operations –

S. no.	Condition	Operation
1.	Initially let both the FFs be in the reset state.	$Q_A Q_B = 0\,0$ initially
2.	After first positive clock edge.	As soon as the first negative clock edge is applied, FF-A will toggle and Q_A will be equal to 1. Q_A is connected to clock input of FF-B. Since Q_A has changed from 1 to 0, it is treated as the positive clock edge by FF-B. There is no change in Q_B because FF-B is a positive edge triggered FF. $Q_A Q_B = 0\,1$ after the first clock pulse.

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Condition	Operation
3. After 2nd positive clock edge.	~~As soon~~ On the arrival of second negative clock edge, FF-A toggles again and Q_A The change in Q_A acts as a positive clock edge for FF-B so it will also toggle and Q_B will be
4. After 3rd positive clock edge.	On the arrival of 3rd positive clock edge, FF-A toggles again. and Q_A become 1 from 0. Since, this is a positive going change, FF-B does not respond to it and remains inactive. So Q_B does not change and continues to be equal to 1. $Q_A Q_B = 11$ after the third clock pulse.
5. After 4th positive clock edge.	On the arrival of 4th positive clock edge. FF-B toggles again and Q_B becomes 1 from 0. This negative change in Q_A act as

Teacher's Signature

Operation

clock pulse for FF-B, Hence it toggles to change Q_A from 1 to 0.
$Q_A Q_B = 00$ after the fourth clock pulse.

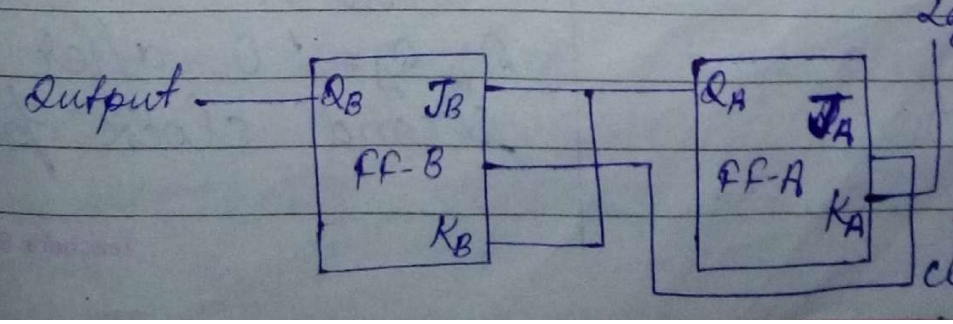
Clock	Counter Output		State Number	Decimal Counter Output
	Q_A	Q_B		
Initially	0	0	—	0
1st	0	1	1	1
2nd	1	0	2	2
3rd	1	1	3	3
4th	0	0	4	0

Synchronous Counters-

If the "clock" pulses are applied to all the flip-flops in a counter simultaneously, then such a counter is called as synchronous counter.

2-bit Synchronous up counter:-

The J_A and K_A inputs of FF-A are tied to logic 1. So FF-A will work as a toggle flip-flop. The J_B and K_B inputs are connected to Q_A of FF-A.



Operations:-

S.no.	Condition	Operation
1.	Initially let both the FFs be in the reset state.	$Q_B Q_A = 00$ initially.
2.	After first negative clock edge.	As soon as the first negative clock edge is applied. FF-A will toggle and Q_A will change from 0 to 1. But at the instant of application of negative clock edge, Q_A, $J_B = K_B = 0$. Hence FF-B will not change its state. So Q_B will remain 0. $Q_B Q_A = 01$ after the first clock pulse.
3.	After 2nd negative clock edge.	On the arrival of second negative clock edge FF-A toggles again and Q_A changes from 0 to 1. $Q_B Q_A = 10$ after the second clock pulse.

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4.	After 3rd negative clock edge.	On application of the third falling clock edge, FF-A will toggle from 0 to 1 but there is no change of state for FF-B. $Q_B Q_A = 11$ after the third clock pulse.
5.	After 4th negative clock edge.	On application of the next clock pulse Q_A will change from 1 to 0 as Q_B will also change from 1 to 0. $Q_B Q_A = 00$ after the fourth clock pulse.

Decade Counters-

It is an asynchronous counter. A decade counter requires resetting to zero when the output count reaches the decimal value of 10 i.e., when Q C B A = 1 0 1 0 and to do this we need to feed this condition back to the reset input. A counter with a count sequence from binary "0000" (BCD = "0") through to "1001" (BCD = "9") is generally referred to as a BCD

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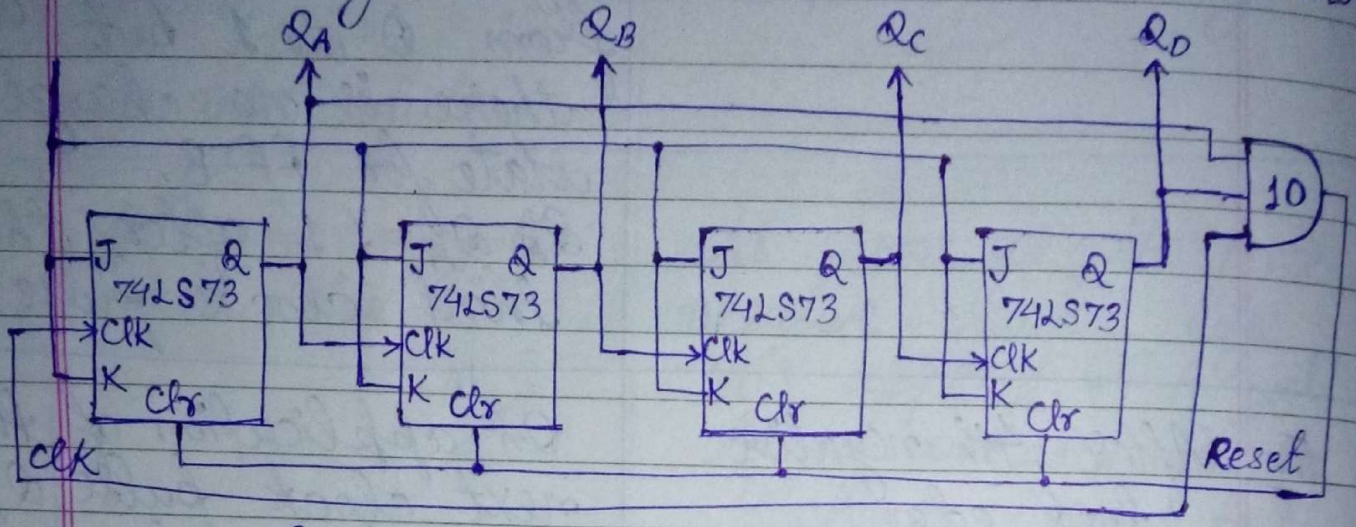
binary-coded-decimal counter because its ten state sequence is that of a BCD code but binary decade counters are more common.



This type of asynchronous counter counts upwards on each trailing edge of the input clock signal starting from 0000 until it reaches an output 1001 (decimal 9).

Both outputs Q_A and Q_B are now equal to logic "1". On the application of the next clock pulse the output from the 74LS10 NAND gate changes state from logic "1" to a logic "0" level.

As the output of the NAND gate is connected to the CLEAR(Clr) inputs of all the 74LS73 J-K flip-flops, this signal causes all of the Q outputs to be reset back to binary 0000 on the count of 10.

As outputs Q_A and Q_D are now both equal to logic "0" as the flip-flop's has just been reset, the output of

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the NAND gate returns back to a logic level "1" and the counter restarts again from 0000. We now have a decade or modulo-10-up-counter.

Decade Counter Truth Table-

Clock Count	Output bit pattern Q_D	Q_C	Q_B	Q_A	Decimal value
1	0	0	0	0	0
2	0	0	0	1	1
3	0	0	1	0	2
4	0	0	1	1	3
5	0	1	0	0	4
6	0	1	0	1	5
7	0	1	1	0	6
8	0	1	1	1	7
9	1	0	0	0	8
10	1	0	0	1	9
11	~~Clock~~ Counter reset its outputs back to zero.				

By using the same idea of truncating counter output sequences, the above circuit could easily be adapted to other counting cycles be simply changing the connection to the inputs of the NAND gate or by using other logic gate combinations.

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BCD Counter-

A BCD counter is a special type of a digital counter. which can count to ten on the application a clock signal.

To make a digital counter which counts from 1 to 10, we need to have the counter count only the binary numbers 0000 to 1001.

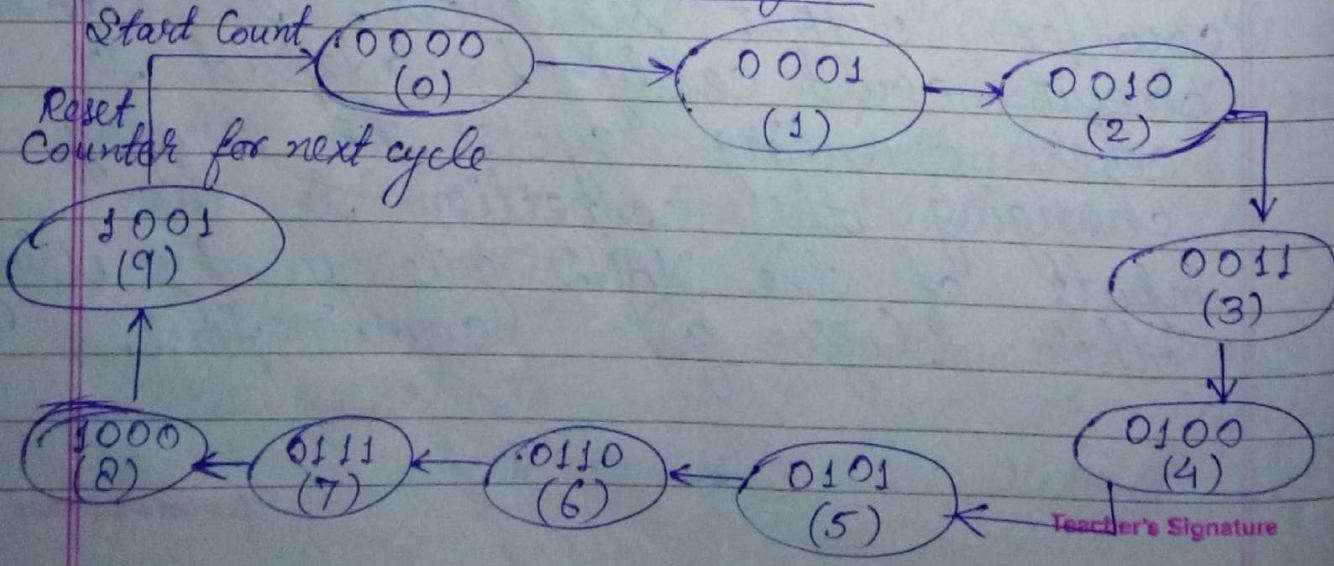
This is from 0 to 9 in decimal.

Digital Counters count upwards from zero to some pre determined count value on the application of a clock signal.

Once the count value is reached, resulting them returns the counter back to zero to start again.

A decade counter counts in a sequence of ten and then returns back to zero after the count of nine.

BCD Counter State Diagram-



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BCD Counter-

A counter which resets after ten counts with a divide-by-10 count sequence from binary 0000 (decimal "0") through to 1001 (decimal "9") is called a binary-coded-decimal counter or BCD counter. It is called a BCD counter because its ten state sequence is that of a BCD code and does not have a regular pattern. Example of ~~BCD~~ Decimal to BCD number.

Decimal	BCD
0	0000
9	1001

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Difference between Asynchronous and Synchronous counter.

Asynchronous	Synchronous
(i) Flip-flops are connected in such a way that output of first flip-flop drives the clock of next flip-flop.	(i) There is no connection between output of first flip-flop and clock of next flip-flop.
(ii) Flip-flops are not clocked simultaneously.	(ii) Flip-flops are clocked simultaneously.
(iii) Circuit is simple for more number of states	(iii) Circuit becomes complicated as number of states increases.
(iv) Speed is slow as clock is propagated through number of states.	(iv) Speed is high as clock is given at a same time.
(v) Asynchronous counter are also known as "Ripple Counter" because of the way the clock pulses or ripples its way through the flip-flop.	

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