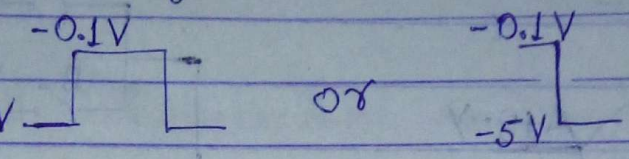
25-01-2017
Wednesday

Unit-I

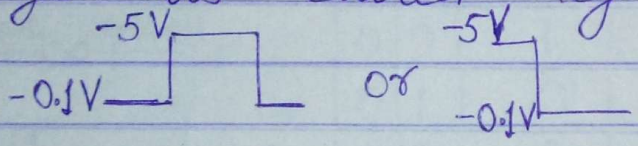
Positive & Negative Logic-

Low - 0
High - 1



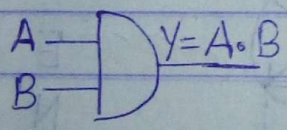
The system in which most positive voltage shows high state (1) & most negative voltage (0) is called positive logic system.

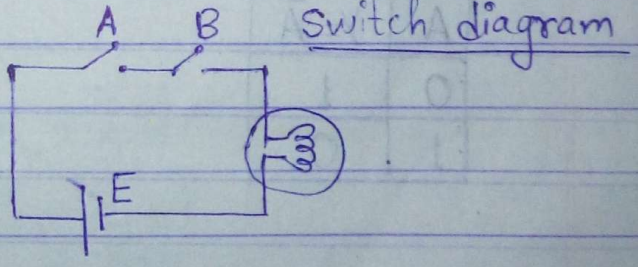
The system in which most negative voltage shows high state & most positive voltage is called negative logic system.



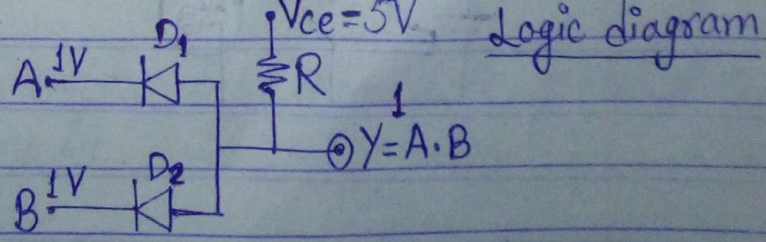
Logic Gates-

(1) AND Gate-

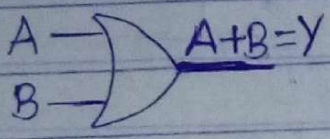


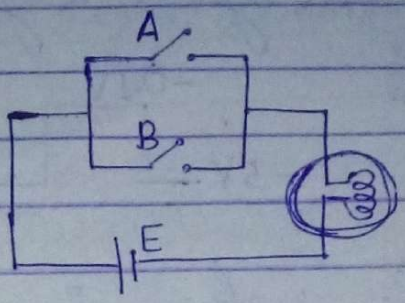


A	B	A.B=Y
0	0	0
0	1	0
1	0	0
1	1	1

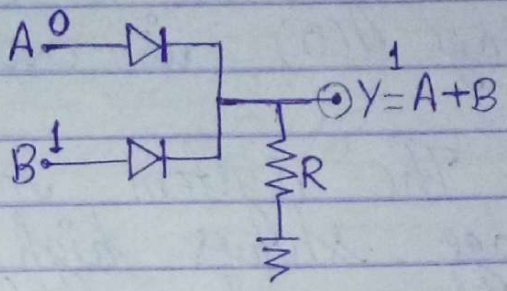


(2) OR Gate –

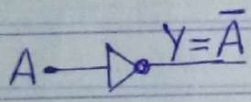




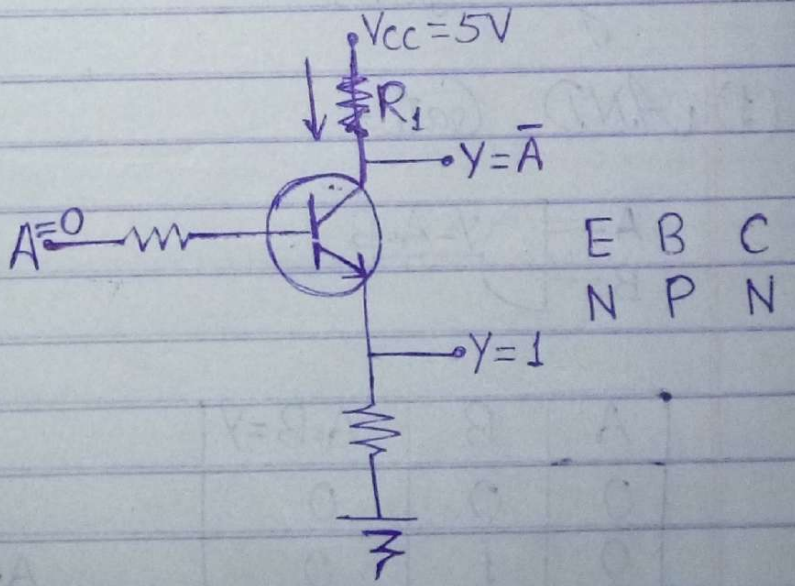
A	B	A+B=Y
0	0	0
0	1	1
1	0	1
1	1	1

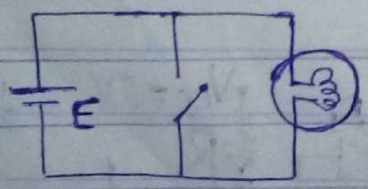


(3) NOT Gate –

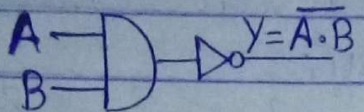


A	Y=Ā
0	1
1	0

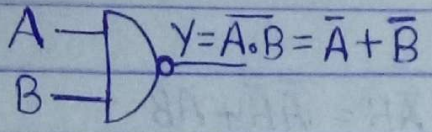




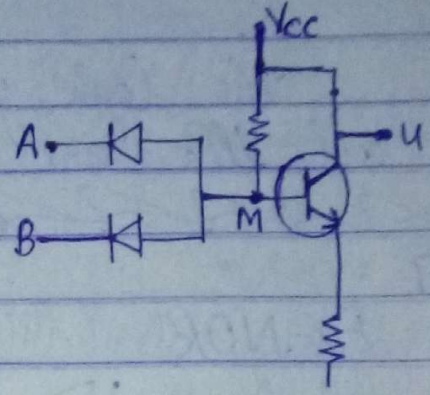
(4.) NAND (NOT + AND) –



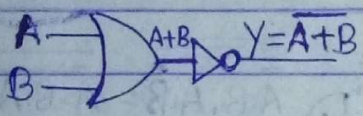
or



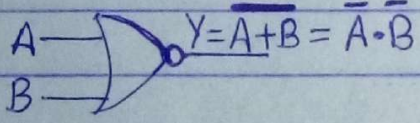
A	B	Y = $\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0



NOR Gate –

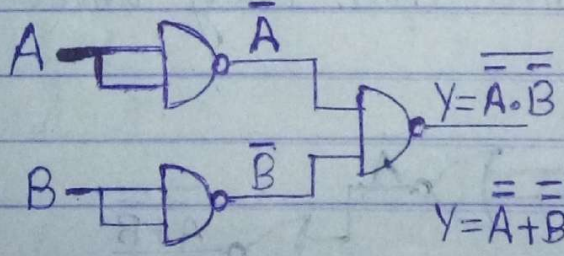


or



A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

(i)

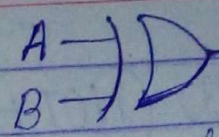


Y = (A + B) [OR Gate]

Note: Logic Gates are formed by diodes & transistors.
3 NAND gates make 1 OR gate.

Saturday
27-01-2017

Exclusive-OR-Gate (EX-OR Gate)

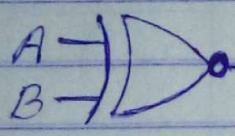


$Y = A \oplus B$
$= A\bar{B} + \bar{A}B$

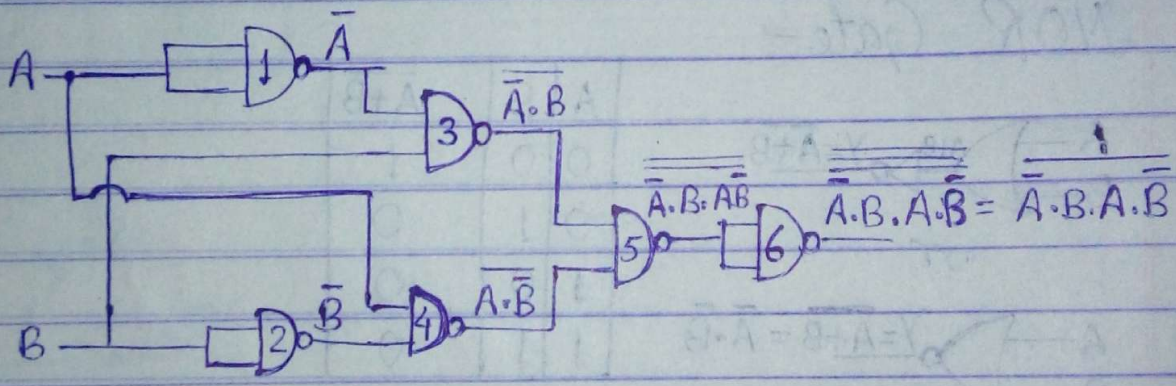
The logic gate which gives low state when all I/Ps are in same state.

27-01-2017
Saturday

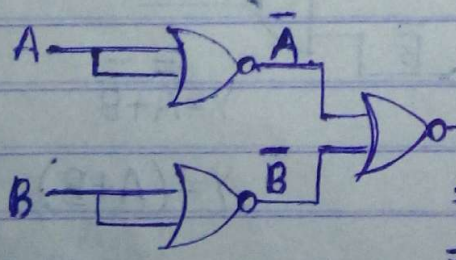
EX-NOR



$Y = \overline{A \oplus B} = \overline{A\bar{B} + \bar{A}B} = \bar{A}\bar{B} + AB$



Q.- Make an AND Gate using three NOR Gates



$= \bar{\bar{A}} \cdot \bar{\bar{B}}$ (By De-Morgan's law)
$= A \cdot B$

Boolean Algebra-

① Commutative Law-
- (i) $A+B=B+A$
- (ii) $A \cdot B = B \cdot A$

② Associative Law-
- (i) $A+(B+C)=(A+B)+C$
- (ii) $A \cdot (B \cdot C)=(A \cdot B) \cdot C$

③ Distributive Law-
- (i) $A \cdot (B+C) = A \cdot B + A \cdot C$

④ Complementry Law-
- (i) $\bar{\bar{A}} = A$

⑤ Laws for OR-operation
- (i) $1+A=1$
- (ii) $0+A=A$
- (iii) $A+A=A$
- (iv) $A+\bar{A}=1$
- (v) $\bar{A}+\bar{A}=\bar{A}$

⑥ Laws for AND-Operation
- (i) $A \cdot 0 = 0$
- (ii) $A \cdot 1 = A$
- (iii) $A \cdot A = A$
- (iv) $A \cdot \bar{A} = 0$
- (v) $\bar{A} \cdot \bar{A} = \bar{A}$
- (vi) $\bar{A} \cdot 0 = 0$
- (vii) $\bar{A} \cdot 1 = \bar{A}$

⑦ Absorption Law-
- (i) $A+AB = A(1+B) = A$
- (ii) $A+\bar{A}B = A(1+B)+\bar{A}B$
  $= A+AB+\bar{A}B$
  $= A+(A+\bar{A})B = A+B$
- (iii) $\bar{A}+AB = \bar{A}(1+B)+A \cdot B$
  $= \bar{A}+\bar{A}B+AB$
  $= \bar{A}+B(A+\bar{A})$
  $= \bar{A}+B$
- (iv) $(A+B)(A+C)$ ~~$= A \cdot A +$~~
  $= A \cdot A + A \cdot C + A \cdot B + B \cdot C$
  $= A(1+C)+A \cdot B+B \cdot C$
  $= A + AB + BC$
  $= A(1+B)+BC$
  $= A + BC$.

⑧ De-Morgan's Law-
- (i) $\overline{A+B} = \bar{A} \cdot \bar{B}$
- (ii) $\overline{A \cdot B} = \bar{A}+\bar{B}$

MINTERM-

A	B	C	MINTERM
0	0	0	$\bar{A}\bar{B}\bar{C}$
0	0	1	$\bar{A}\bar{B}C$
0	1	0	$\bar{A}B\bar{C}$
0	1	1	$\bar{A}BC$
1	0	0	$A\bar{B}\bar{C}$
1	0	1	$A\bar{B}C$
1	1	0	$AB\bar{C}$
1	1	1	ABC

Definition-
MINTERM is the product term in which all the variables are present in either in complement form or uncomplement form.

① Minterm produces '1' (High State) for corresponding combination.
② Minterm produces '0' (Low State) for all other combinations.

MAXTERM-

A	B	C	MAXTERM
0	0	0	$A+B+C$
0	0	1	$A+B+\bar{C}$
0	1	0	$A+\bar{B}+C$
0	1	1	$A+\bar{B}+\bar{C}$
1	0	0	$\bar{A}+B+C$
1	0	1	$\bar{A}+B+\bar{C}$
1	1	0	$\bar{A}+\bar{B}+C$
1	1	1	$\bar{A}+\bar{B}+\bar{C}$

Definition
MAXTERM is the sum term in which all the variables are present in either in complement or uncomplement form.

~~Sum of Produ~~

① MAXTERM produces '0' (Low State) for corresponding combinations.
② MAXTERM produces '1' (High State) for all other combinations.

Sum of Product (SOP) Term-

Sum of Product is the term in which sum of all product terms/minterm is called SOP.

e.g.→ $A\bar{B}C + \bar{A}BC + \bar{A}\bar{B}$

$A\bar{B}C + \bar{A}BC + \bar{A}\bar{B}(C+\bar{C})$ (By Absorption Law)

$A\bar{B}C + \bar{A}BC + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}$ (By Distributive Law)

$\underset{111}{A\bar{B}C} + \underset{011}{\bar{A}BC} + \underset{010}{\bar{A}\bar{B}\bar{C}}$

Product of Sum (POS) Term/Form-

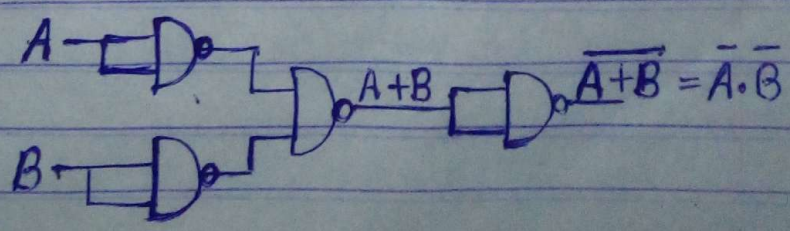
Product of all sum terms/maxterms is called POS.

e.g.→ $\underset{001}{(A+B+\bar{C})} \cdot \underset{011}{(A+\bar{B}+\bar{C})} \cdot \underset{100}{(\bar{A}+B+C)}$

$(A+B+\bar{C}) \cdot (A+\bar{B}+\bar{C}) \cdot (\bar{A}+B+C\bar{C})$ (by absorption law)

$(A+B)(A+C) = (A+BC)$ (by absorption law)

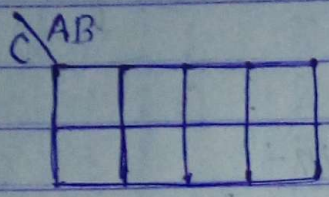
Q.→ Design NOR Gate using only NAND Gate. →



Thursday
02-02-17

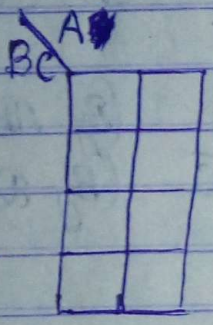
KARNAUGH MAP (K-MAP) –

2^{n} variable

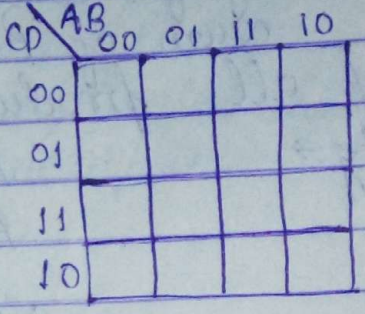


Leftmost + Rightmost
Uppermost + Lowermost

or



Adjacent Cells



A B C	A B C
0 1 0	0 1 1
2	3

$1\times2^{2}+0\times2^{1}+1\times2^{0}=5$
$4+0+1=5$

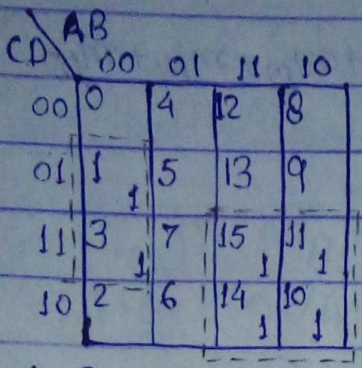
m = MINTERM
M = MAXTERM

$Y=\Sigma(m_1, m_3, m_{10}, m_{11}, m_{14}, m_{15})$ using K-Map.

$A\bar{B}CD+\bar{A}\bar{B}CD+A\bar{B}\bar{C}\bar{D}+\bar{A}\bar{B}CD+\bar{A}\bar{B}\bar{C}D+ABC\bar{D}+ABCD$

1011	0011	1010	0011	0001	1110	1111
11	3	10		1	14	15

000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7



Adjacent Cells
Cell - 10, 11, 14, 15

Cell - 1, 3

$Y_2 = \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}CD$

$= \bar{A}\bar{B}D(\bar{C}+C)$

$Y_2 = \bar{A}\bar{B}D$

$Y_1 = A\bar{B}\bar{C}\bar{D} + A\bar{B}CD + AB\bar{C}\bar{D} + ABCD$

$= A\bar{B}C(D+\bar{D}) + ABC(D+\bar{D})$

$= A\bar{B}C + ABC = AC(\bar{B}+B)$

$Y_1 = AC$

$Y = Y_1 + Y_2$

$Y = \bar{A}\bar{B}D + AC$

Conversion of SOP into SSOP. (Standard SOP)

Q. $\bar{A}BC(D+\bar{D}) + \bar{A}BC(D+\bar{D}) + \bar{A}BC\bar{D} + A\bar{B}\bar{C}D + A\bar{B}C\bar{D} + \bar{A}\bar{B}CD + A\bar{B}C + \bar{A}B$
~~$\bar{A}BC + \bar{A}BC\bar{D} + A\bar{B}\bar{C}D + \bar{A}\bar{B}CD + A\bar{B}C(D+\bar{D}) + \bar{A}B(C+\bar{C})$~~

$= \bar{A}BCD + \bar{A}BC\bar{D} + \bar{A}BCD + \bar{A}BC\bar{D} + \bar{A}BC\bar{D} + A\bar{B}\bar{C}D + A\bar{B}\bar{C}D + \bar{A}\bar{B}CD$
$+ A\bar{B}C(D+\bar{D}) + \bar{A}B(C+\bar{C})$

$= \bar{A}BCD + \bar{A}BC\bar{D} + \bar{A}BCD + \bar{A}BC\bar{D} + \bar{A}BC\bar{D} + A\bar{B}\bar{C}D + A\bar{B}\bar{C}D + \bar{A}\bar{B}CD$
$+ A\bar{B}CD + A\bar{B}C\bar{D} + \bar{A}BC + \bar{A}BC$

$= \bar{A}BCD + \bar{A}BC\bar{D} + \bar{A}BCD + \bar{A}BC\bar{D} + \bar{A}BC\bar{D} + A\bar{B}\bar{C}D + A\bar{B}\bar{C}D + \bar{A}\bar{B}CD$
$+ A\bar{B}CD + A\bar{B}C\bar{D} + \bar{A}BC(D+\bar{D}) + \bar{A}BC(D+\bar{D})$

$= \bar{A}BCD + \bar{A}BC\bar{D} + \bar{A}BCD + \bar{A}BC\bar{D} + \bar{A}BC\bar{D} + A\bar{B}\bar{C}D + A\bar{B}\bar{C}D + \bar{A}\bar{B}CD$
$+ A\bar{B}CD + A\bar{B}C\bar{D} + \bar{A}BCD + \bar{A}BC\bar{D} + \bar{A}B\bar{C}D + \bar{A}B\bar{C}\bar{D}$

$= \bar{A}BCD + \bar{A}BC\bar{D} + A\bar{B}\bar{C}D + \bar{A}\bar{B}CD + A\bar{B}CD + A\bar{B}C\bar{D} + \bar{A}B\bar{C}D + \bar{A}B\bar{C}\bar{D}$

$= \bar{A}BC(D+\bar{D}) + A\bar{B}D(\bar{C}+C) + \bar{B}CD(\bar{A}+A) + \bar{A}B\bar{C}(D+\bar{D})$

$= \bar{A}BC + A\bar{B}D + \bar{B}CD + \bar{A}B\bar{C} = \bar{A}B(C+\bar{C}) + \bar{B}D(A+C)$

$= \bar{A}B + \bar{B}D(A+C)$

Friday
03-02-17

$Y = \Sigma m\,(0,1,3,6,8,9,10,12,14,15)$

$= m_0 + m_1 + m_3 + m_6 + m_8 + m_9 + m_{10} + m_{12} + m_{14} + m_{15}$

$= \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}CD + \bar{A}B\bar{C}\bar{D}$

↓

$A+B+C+D$

MINTERM –

CD \ AB	00	01	11	10
00	0 1	4 1	12 1	8 1
01	1 1	5	13	9 1
11	3 1	7	15 1	11
10	2	6 1	14 1	10 1

Quad 1: $(m_0 + m_1 + m_8 + m_9)$

Quad 2: $(m_8 + m_{10} + m_{12} + m_{14})$

Pair 1: $(m_1 + m_3)$

Pair 2: $(m_6 + m_{14})$

Pair 3: $(m_{14} + m_{15})$

Quad 1: $Y_1 = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D$

$= \bar{A}\bar{B}\bar{C}(\bar{D}+D) + A\bar{B}\bar{C}(\bar{D}+D)$

$= \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} = \bar{B}\bar{C}(\bar{A}+A) = \bar{B}\bar{C}.$

Quad 2: $Y_2 = A\bar{B}\bar{C}\bar{D} + A\bar{B}CD + AB\bar{C}\bar{D} + ABC\bar{D}$

~~$= A\bar{B}\bar{C}\bar{D} + AB\bar{C}\bar{D} + AB\bar{C}D + ABC\bar{D}$~~

~~$= A\bar{C}\bar{D}(\bar{B}+B) + AB\bar{D}(\bar{C}+C)$~~ $= A\bar{B}\bar{D}(\bar{C}+C) + AB\bar{D}(C+\bar{C})$

$= A\bar{B}\bar{D} + AB\bar{D} = A\bar{D}$ ~~$(B+\bar{B})$~~

~~MAXTERM~~

Pair 1: $Y_3 = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D = \bar{A}\bar{B}\bar{D}$ $= \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}CD$

$= \bar{A}\bar{B}D$

Pair 2: $Y_4 = \bar{A}BC\bar{D} + ABC\bar{D} = BC\bar{D}$

Pair 3: $Y_5 = ABC\bar{D} + ABCD = ABC$

$Y = Y_1 + Y_2 + Y_3 + Y_4 + Y_5 = \bar{B}\bar{C} + A\bar{D} + \bar{A}\bar{B}D + BC\bar{D} + ABC$

$Y = \Pi_M (0,1,3,6,8,9,10,12,14,15)$

$= M_0 \cdot M_1 \cdot M_3 \cdot M_6 \cdot M_8 \cdot M_9 \cdot M_{10} \cdot M_{12} \cdot M_{14} \cdot M_{15}$

$Y_1 = M_0 \cdot M_1 \cdot M_8 \cdot M_9$

$= (A+B+C+D).(A+B+C+\bar{D}).(\bar{A}+B+C+D).(\bar{A}+B+C+\bar{D})$

$(A+B)(A+C) = A+BC$ (Absorption Law)

$Y_1 = [(A+B+C)+D.\bar{D}].[(\bar{A}+B+C)+D\bar{D}]$

$= (A+B+C).(\bar{A}+B+C) = (B+C)$

$Y_2 = (\bar{A}+B+C+D).(\bar{A}+B+\bar{C}+D).(\bar{A}+\bar{B}+C+D).(\bar{A}+\bar{B}+\bar{C}+D)$

$= (\bar{A}+B+D).(\bar{A}+\bar{B}+D) = (\bar{A}+D)$

$Y_3 = (A+B+C+D).(A+B+C+D) = (A+B+\bar{D})$

$Y_4 = (A+\bar{B}+\bar{C}+D).(\bar{A}+\bar{B}+\bar{C}+D) = (\bar{B}+\bar{C}+D)$

$Y_5 = (\bar{A}+\bar{B}+\bar{C}+D).(\bar{A}+\bar{B}+\bar{C}+\bar{D}) = (\bar{A}+\bar{B}+\bar{C})$

$Y = Y_1 \cdot Y_2 \cdot Y_3 \cdot Y_4 \cdot Y_5 = (B+C).(\bar{A}+D).(A+B+\bar{D}).(\bar{B}+\bar{C}+D).(\bar{A}+\bar{B}+\bar{C})$

Don't Care Combination – (x, d, ϕ)

$Y = \Pi_M (0,3,6,10,12) + \Pi_d (1,7,14)$

CD \ AB	00	01	11	10
00	0 1	4	12 1	8
01	1 d	5	13	9
11	3 1	7 d	15	11
10	2 1	6 1	14 d	10 1

Pair 1 $[m_0, m_1]$

$Y_1 = m_0 + m_1$

$= \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D$

$Y_1 = \bar{A}\bar{B}\bar{C}$

Pair 2:

$d(1,7,14)$

d_1, d_7, d_{14}

$(m_3 + m_7)$

$= \bar{A}\bar{B}CD + \bar{A}BCD$

$= \bar{A}CD$

Pair 3: $(m_6 + m_{14})$

$= \bar{A}BC\bar{D} + ABC\bar{D}$

$= BC\bar{D}$

Pair 4: $(m_{14} + m_{10})$

$= ABC\bar{D} + A\bar{B}C\bar{D}$

$= AC\bar{D}$

$Y = \Pi_M (0,1,2,4,5,8,7,9,11,14,15)$

CD \ AB	00	01	11	10
00	0 1	4 1	12 1	8 1
01	1 1	5 1	13	9 1
11	3	7 1	15 1	11 1
10	2 1	6	14 1	10

1	1	1	1
1	1		1
	1	1	1
1		1	

Quad: $Y_1 = m_0 \cdot m_1 \cdot m_4 \cdot m_5 = (A+B+C+D) \cdot (A+B+C+\bar{D}) \cdot (A+\bar{B}+C+D) \cdot (A+\bar{B}+C+\bar{D})$

~~$= ABC$~~ $= [(A+B+C) + D \cdot \bar{D}] \cdot [(A+\bar{B}+C) + D \cdot \bar{D}]$

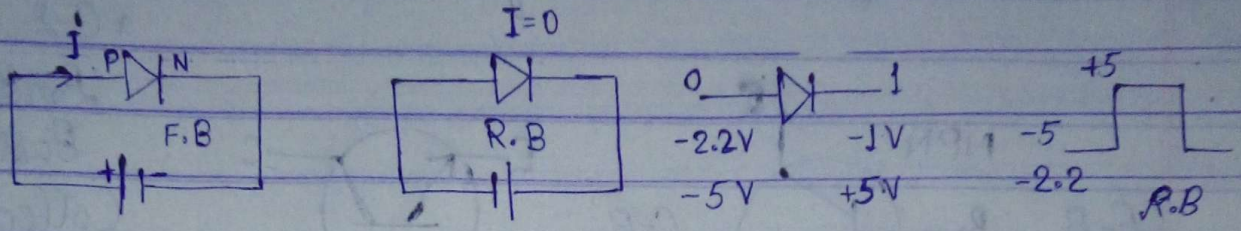
$= (A+B+C) \cdot (A+\bar{B}+C)$

$= [(A+C) + B \cdot \bar{B}]$

$Y_1 = (A+C)$

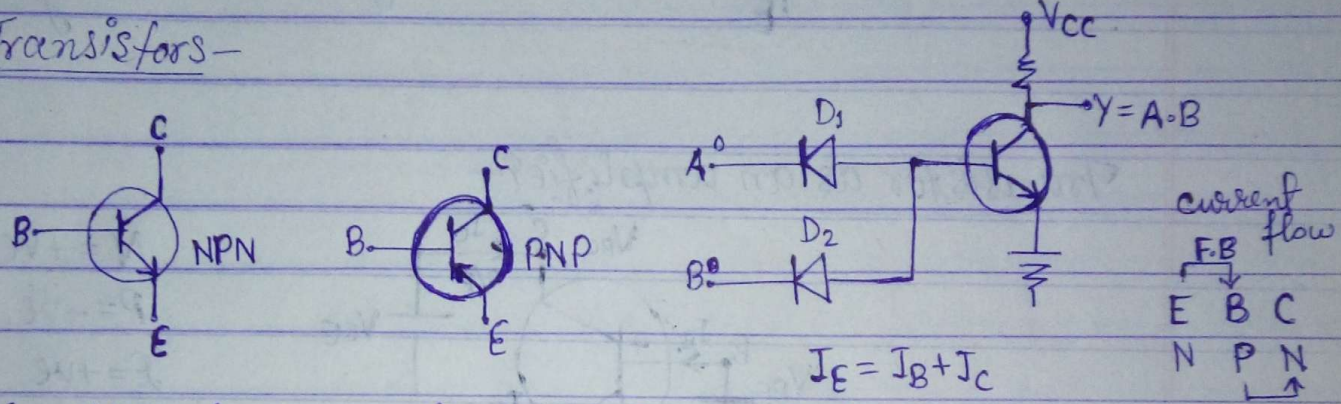
D.I.Y

Diodes –



F.B = Forward Bias , R.B = Reverse Bias

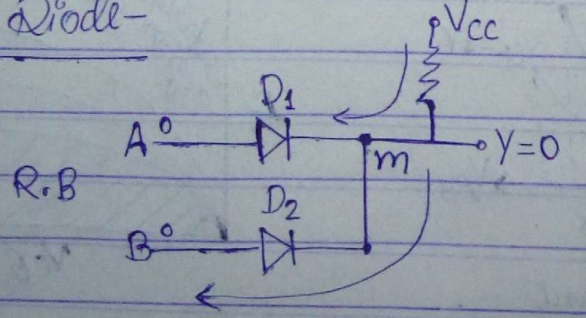
Transistors –



(i) When 'p' at low voltage and 'n' at high voltage diode will be in reverse bias condition, i.e., no current conduction.
(ii) When 'p' at high voltage and 'n' at low voltage diode will be in forward bias i.e., conduction of current.

(i) When E-B junction in forward bias conduction of current.
(ii) When E-B junction in reverse bias no conduction of current.

AND Gate Diode –

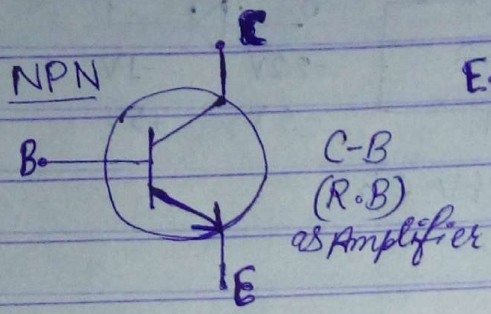


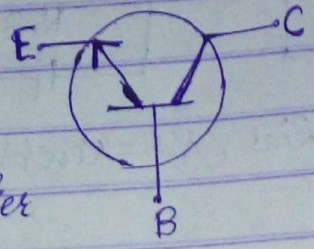
Truth Table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Friday
10-02-17

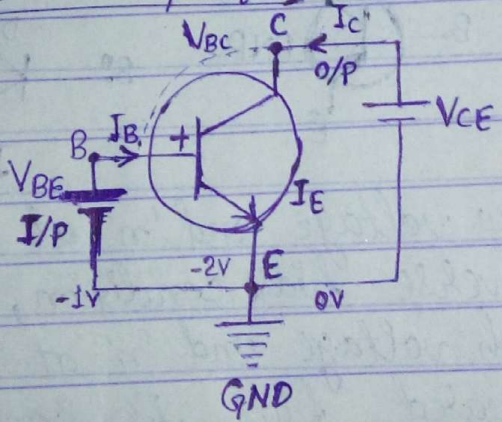
Transistor (BJT) - (Transfer + resistor)





* C-E is better.
Emitter = I/P
Base = Build
Collector = O/P
* E & C are always same

Transistor as an amplifier -

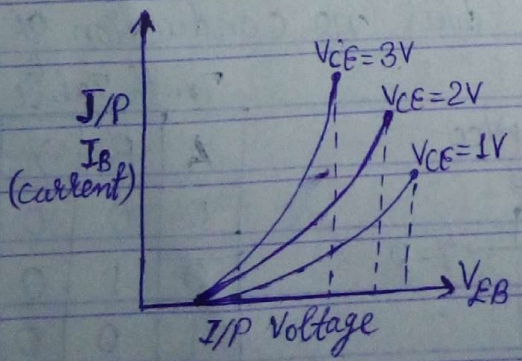


N = +ve
P = -ve
E = +ve
C = -ve

$I_E = I_B + I_C$

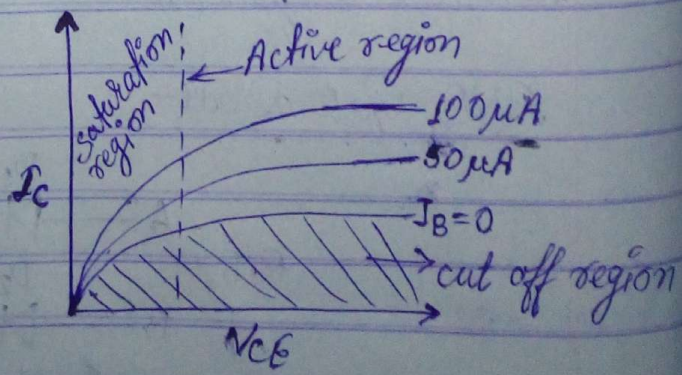
I_E is almost I_C

Input Characteristics -



O/P Voltage = constant.

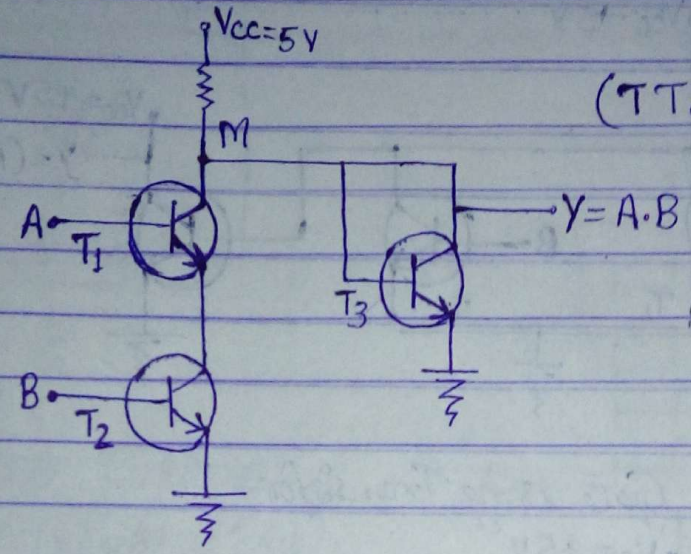
Output Characteristics -



Saturday
11-02-2017

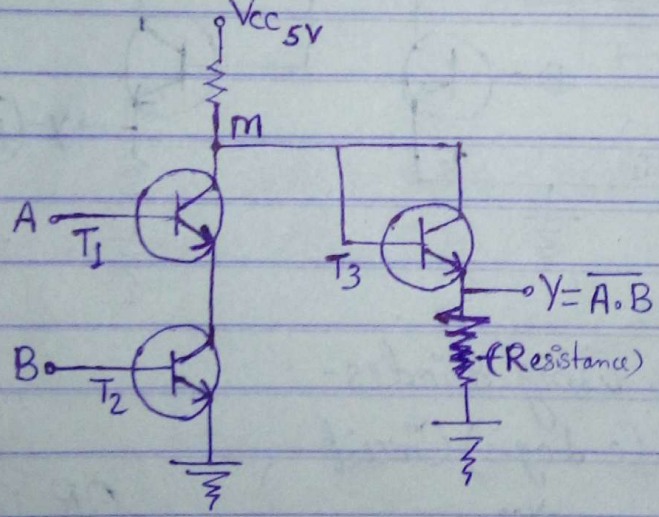
TTL (Transistor-Transistor Logic) Circuit

Make AND Gate using Transistor-

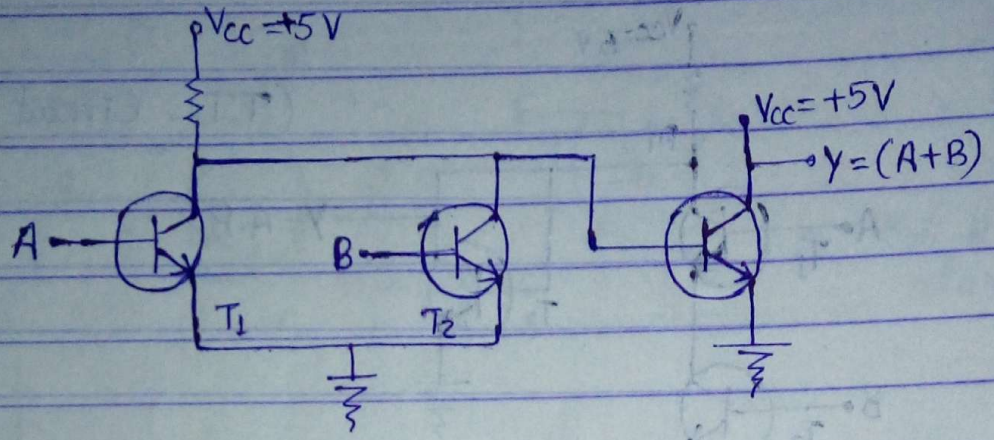


(TTL Circuit)

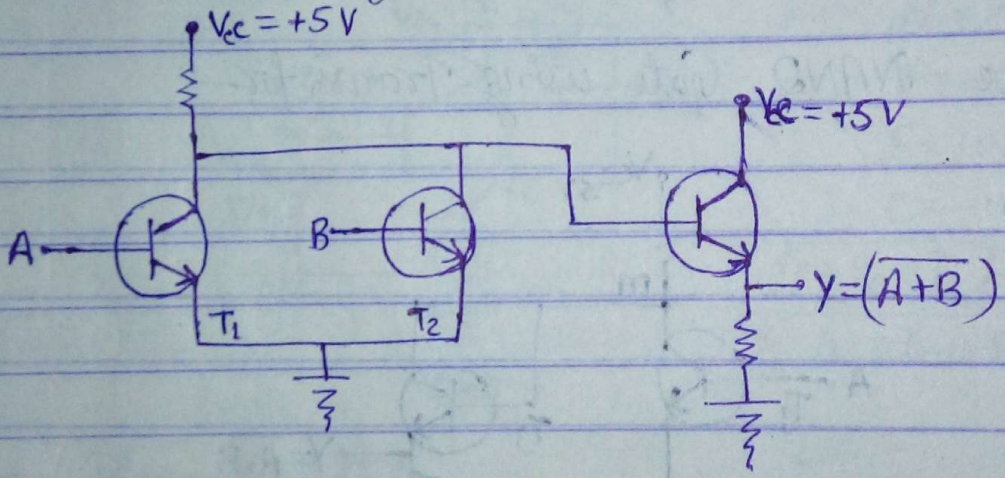
Make NAND Gate using Transistor-



Make OR Gate using Transistor-

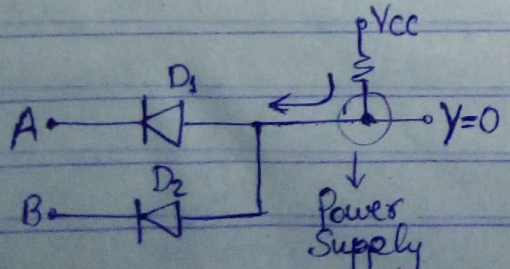


Make NOR Gate using Transistor-

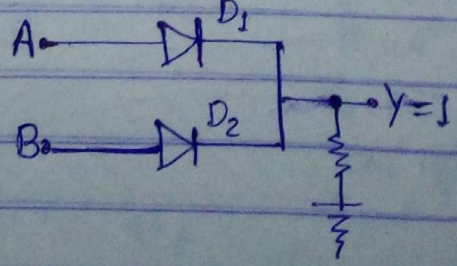


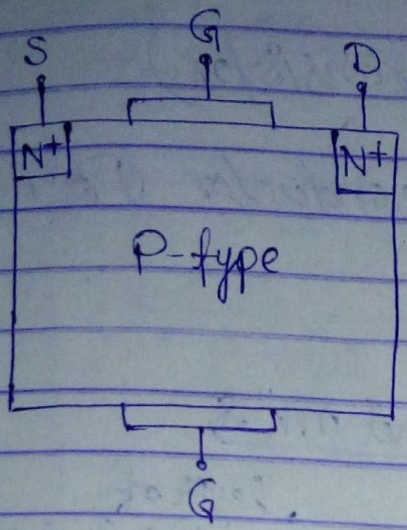
Make AND Gate using Diodes-

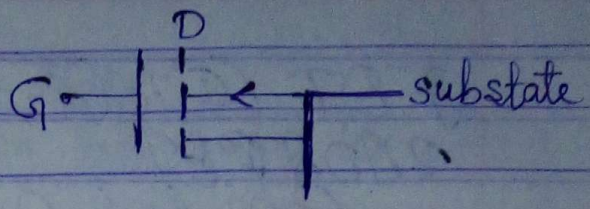
DDL (Diode-Diode Logic) Circuit



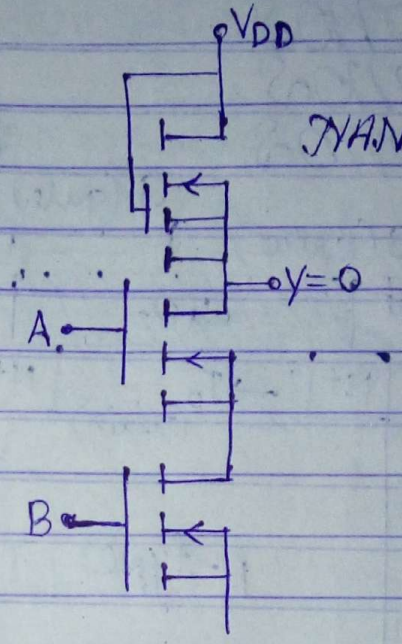
OR Gate







I_D = Drain Current
V_{GS} = -ve (Reverse Bias)
V_{DS} = +ve (Forward Bias)



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

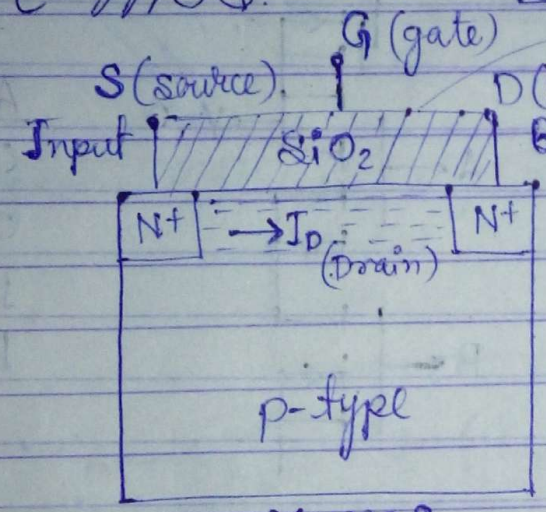
* When G is low then RB. (Zero current flow)
* When G is high then FB.

Saturday
25-03-17

FET (Field Effect Transistor) -
MOSFET
(Metal-Oxide-Semiconductor FET)

1. N-MOS
2. P-MOS
3. C-MOS

N-Channel MOS



layer of SiO_2 (Dielectric)

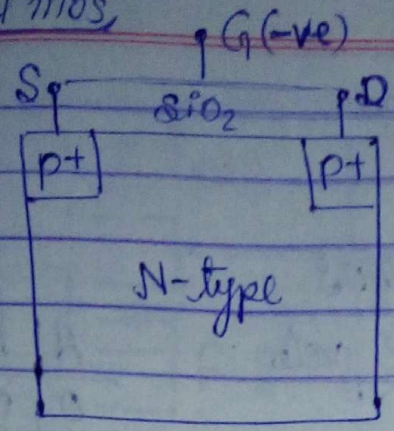
(i) ON-state / Current flow when gate is +ve (1 state)

(ii) OFF-state ($I_D = 0$) when gate is -ve (0 state)

V_{GS} = +ve (I_D)
V_{GS} = -ve ($I_D = 0$)

V_{GS} = Input
V_{DS} = Output
I_D = Drain gate

P-channel MOS

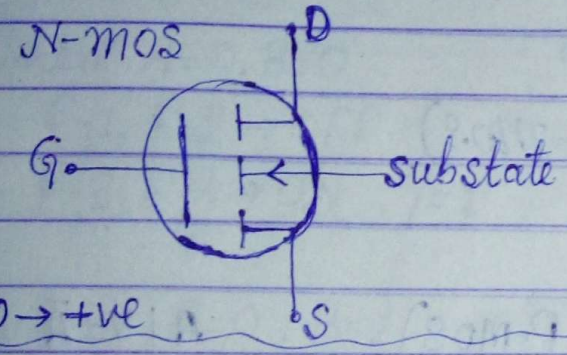


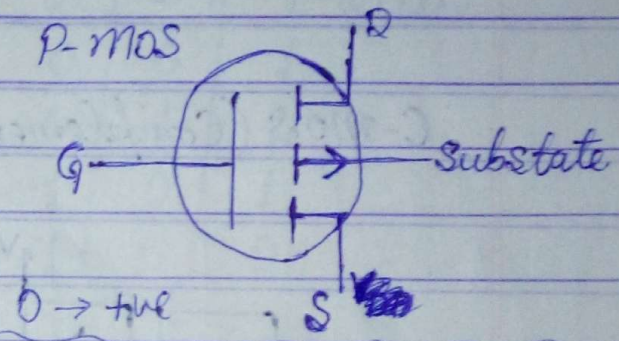
(i) ON-state
when gate is -ve (0 state)

(ii) OFF-state.
when gate is +ve (1 state)

V_{GS} = -ve (I_D)

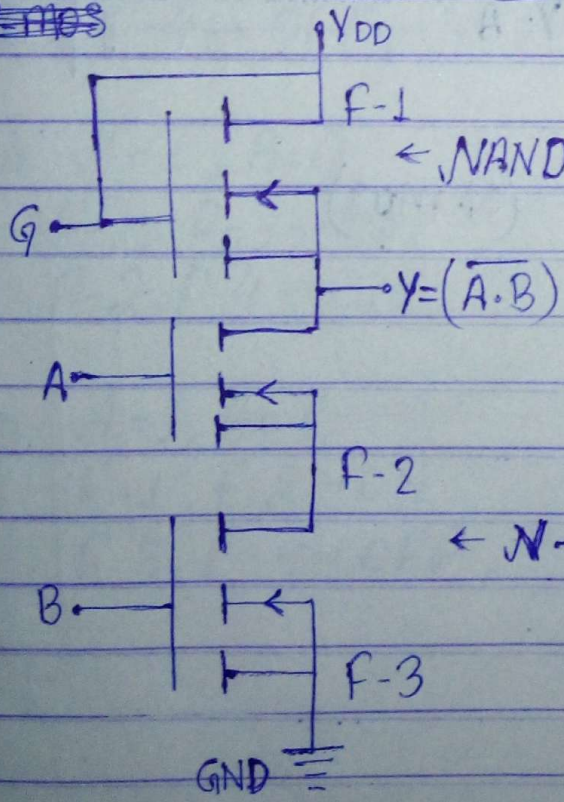
V_{GS} = +ve (I_D = 0)





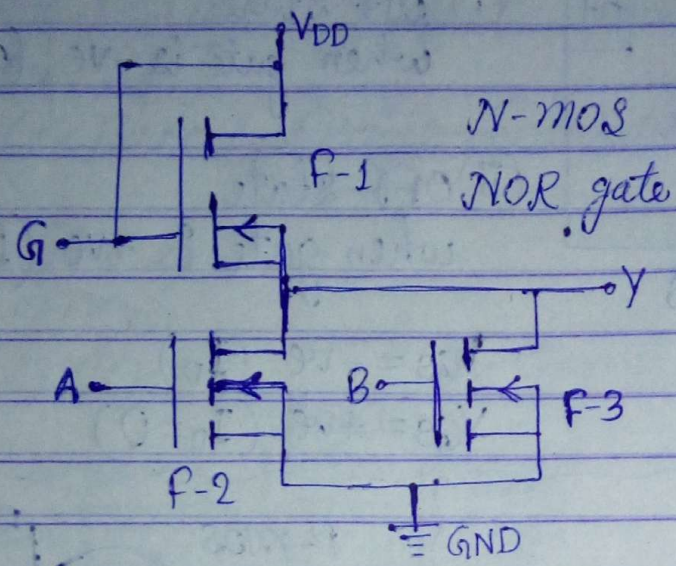
N-MOS NAND Gate –

~~P-MOS~~



A	B	$Y = \overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

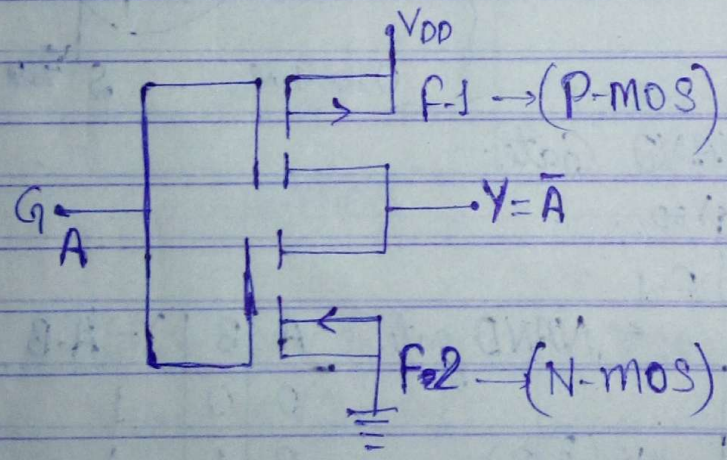
N-MOS NOR Gate -



N-MOS NOR gate

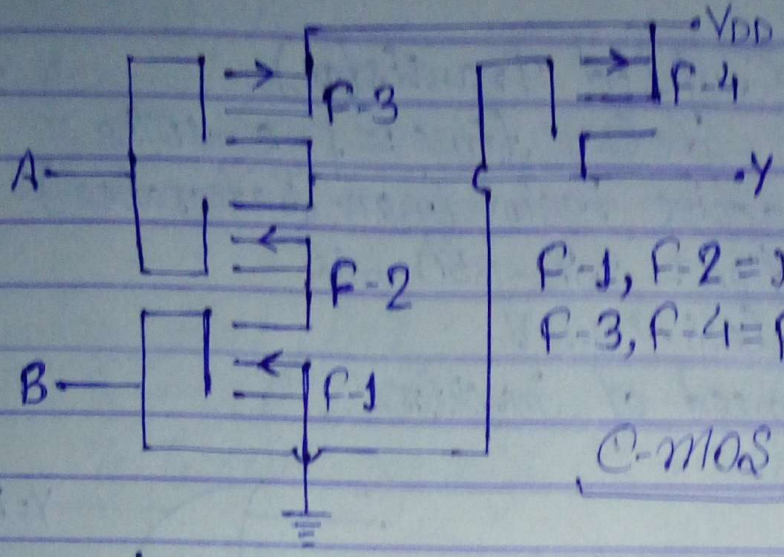
A	B	$Y=\overline{(A+B)}$
0	0	1
0	1	0
1	0	0
1	1	0

C-MOS (Complementary - MOS)



A	$Y=\bar{A}$
0	1
1	0

Wednesday
01-03-17



F-1, F-2 = N-mos
F-3, F-4 = P-mos

C-MOS NAND Gate,

A	B	Y = $\overline{(A \cdot B)}$
0	0	1
0	1	1
1	0	1
1	1	0

(i) when A=0, B=0
F-1, F-2 → OFF
F-3, F-4 → ON, Y=1

(ii) when A=0, B=1
F-1, F-3 → ON
F-2, F-4 → OFF, Y=1

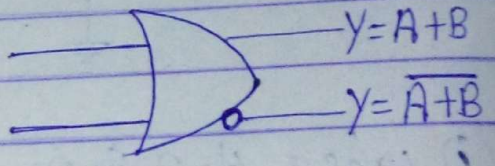
NPN
B=0, OFF
B=1, ON

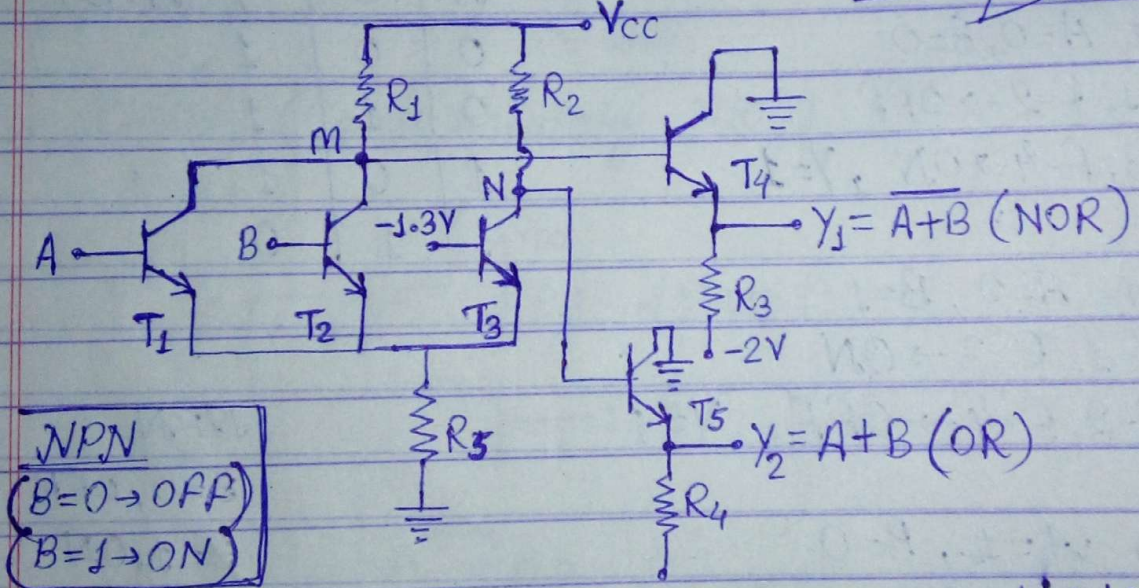
(iii) when A=1, B=0
F-1, F-3 → OFF
F-2, F-4 → ON; Y=1

(iv) when A=1, B=1
F-1, F-2 → ON
F-3, F-4 → OFF, Y=0.

ECL (Emitter Coupled Transistor)

1.) Fast operation - delay time $\simeq 1ns = 10^{-9}s$
2.) It works in active region (non-saturated)
3.) Power dissipation $\simeq 200-350$ mW
4.) Noise margin less $\sim 0.2V$
5.) There is no need of inverter.
6.) 0 state $= -1.7V$
1 state $= -0.8V$





NPN
(B=0 → OFF)
(B=1 → ON)

(i) when A=0, B=0
$T_1, T_2 \rightarrow$ OFF, M-High ($T_4 \rightarrow$ ON) $Y_1=1$
$T_3 \rightarrow$ ON, N-Low ($T_5 \rightarrow$ OFF) $Y_2=0$.

(ii) when A=0, B=1
$T_1, T_3 \rightarrow$ OFF, M-Low ($T_4 \rightarrow$ OFF) $Y_1=0$
$T_2 \rightarrow$ ON, N-Low ($T_5 \rightarrow$ ON) $Y_2=1$

A	B	Y_1	Y_2
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

(iii) when $A=1, B=0$

$T_2, T_3 \rightarrow$ OFF, $M \rightarrow$ Low ($T_4 \rightarrow$ OFF) $Y_1=0$

$T_1 \rightarrow$ ON, $N \rightarrow$ High ($T_5 \rightarrow$ ON) $Y_2=1$

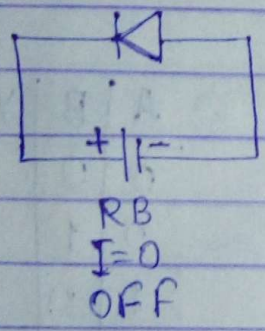
(iv) when $A=1, B=1$

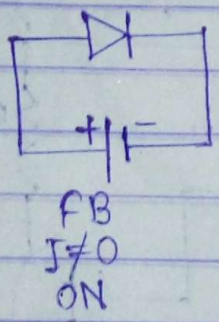
$T_3 \rightarrow$ OFF, $M \rightarrow$ Low ($T_4 \rightarrow$ OFF) $Y_1=0$

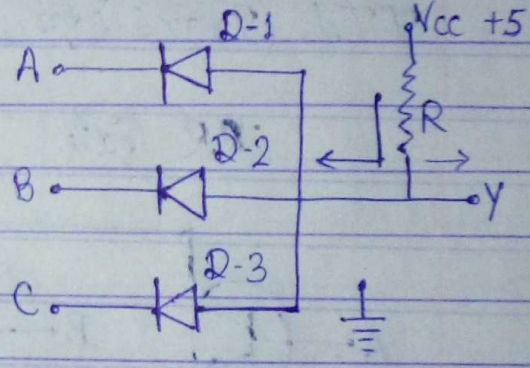
$T_1, T_2 \rightarrow$ ON, $N \rightarrow$ High ($T_5 \rightarrow$ ON) $Y_2=1$

Thursday
02-03-17

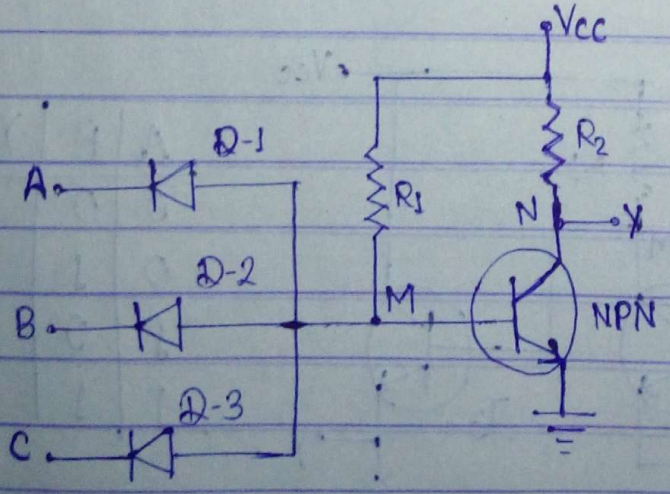
DTL (Diode Transistor Logic)



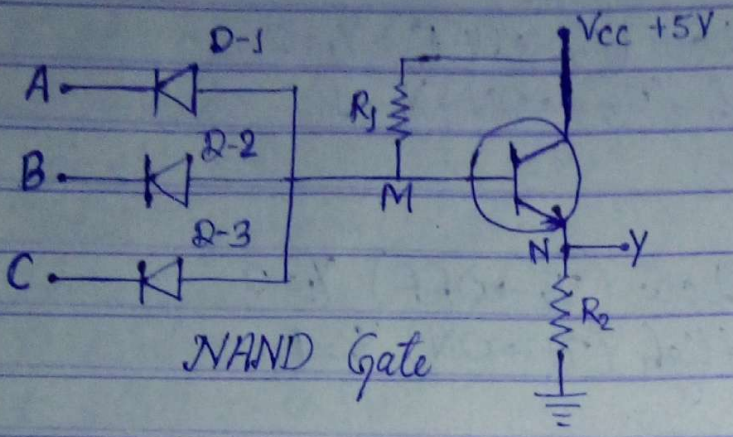




A	B	C	Y=A·B·C
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1



AND Gate

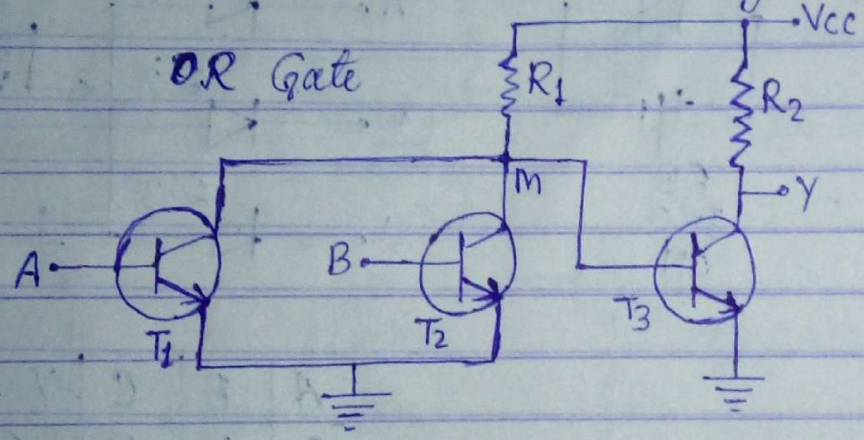


NAND Gate

A	B	C	$Y = \overline{A \cdot B \cdot C}$
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

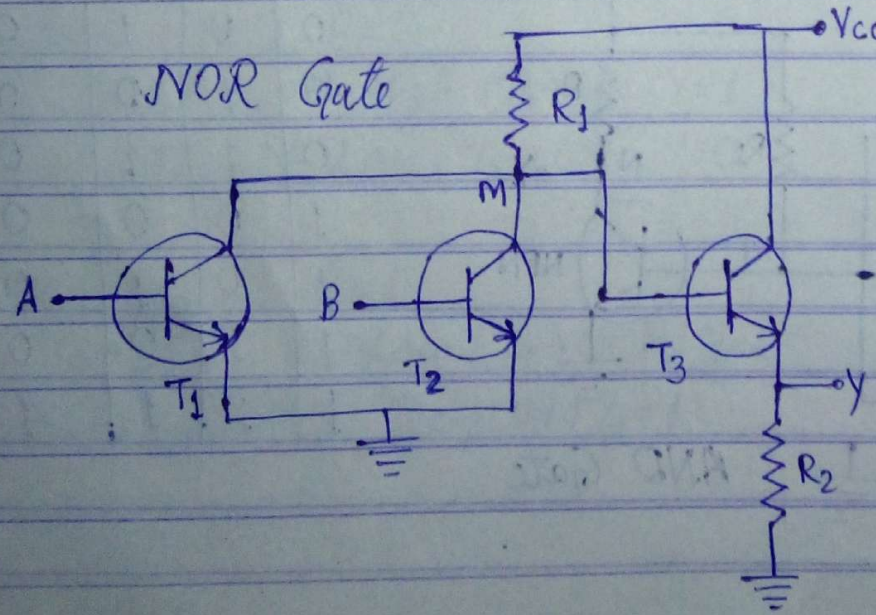
TTL (Transistor Transistor Logic)

OR Gate



A	B	$Y = A+B$
0	0	0
0	1	1
1	0	1
1	1	1

NOR Gate



A	B	$Y = \overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

TTL-Series –

	Version	Abbreviation	Propagation Time (nS)	Power Dissipation (mW)	Fan-out
1.	Standard	TTL	10	10	10
2.	Low power	LTTL	33	1	10
3.	High Speed	HTTL	6	22	10
4.	Schotkey	STTL	3	19	10
5.	Low power Schotkey	LSTTL	9.5	2	10

Unit - III

Combinational Circuits -

The digital circuits in which the output depend upon present input combination not on any past information.

Multiplexer (MUX): Many-into-one

(Several inputs → one output.)

The combinational circuit which select information from several source and transmit it on single output line is called multiplexer. It is also called data selector.

The multiplexers are represented by n-to-1 mux where n is number of data inputs. (They are represented by $D_0, D_1, D_2 \dots D_{n-1}$)

The number of select signals represented by $n = 2^m$ and m = number of select signals ($S_0, S_1, \dots S_{m-1}$)

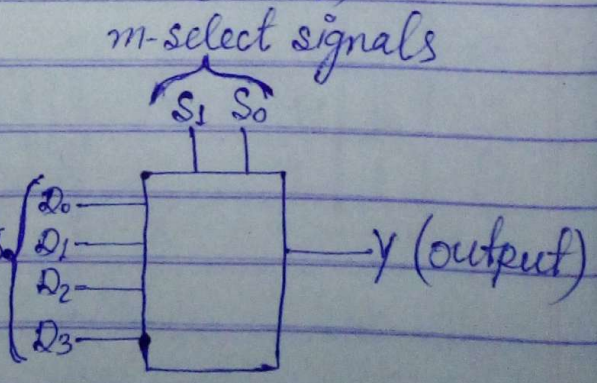
Example -

For 4-to-1 MUX
there are 4-data inputs (D_0, D_1, D_2, D_3)
No. of select signals -

$4 = 2^m \Rightarrow m = 2$ (S_0, S_1)

Table for 4-to-1 MUX -

S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3



$Y = D_0 \bar{S}_1 \bar{S}_0 + D_1 \bar{S}_1 S_0 + D_2 S_1 \bar{S}_0 + D_3 S_1 S_0$

8-to-1 MUX (IC-74151)-

There are 8 data inputs ($D_0, D_1, D_2, D_3, D_4, D_5, D_6, D_7$)

$8 = 2^m \Rightarrow m = 3$

* Select signals – S_0, S_1, S_2

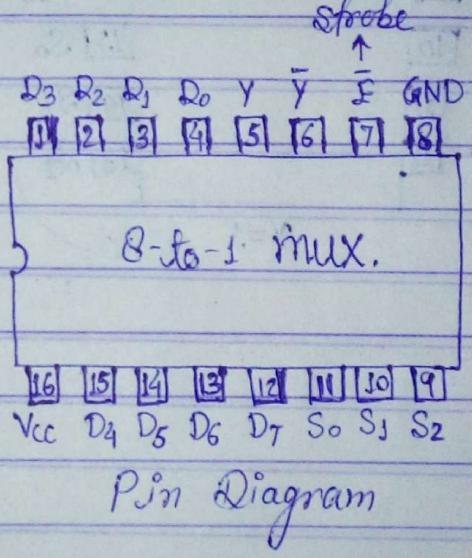
Enable/Strobe input ($\bar{E}$).

$\bar{E} = 1$ (OFF)

$\bar{E} = 0$ (ON)

It produce output, inverted output.

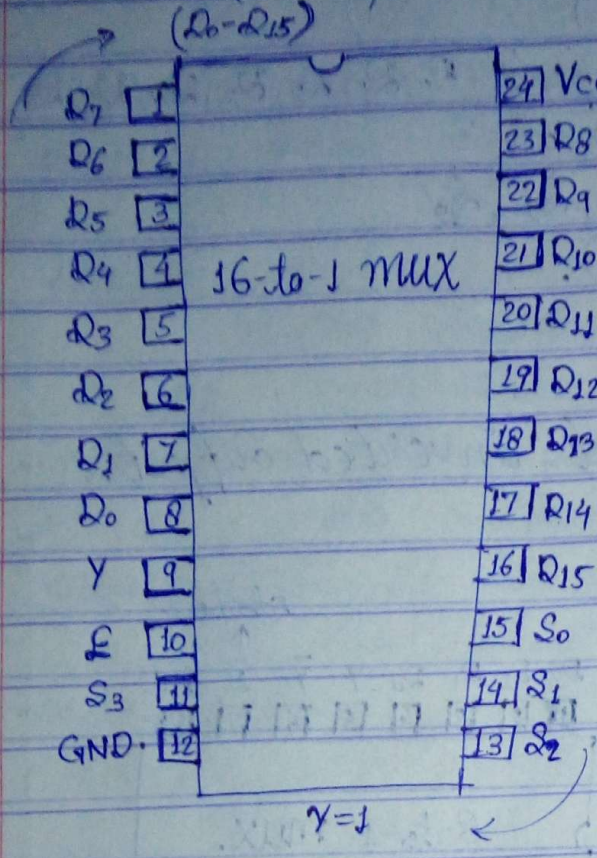
$\bar{E}$	S_2	S_1	S_0	Y	$\bar{Y}$
1	X	X	X	1	0
0	0	0	0	D_0	$\bar{D}_0$
0	0	0	1	D_1	$\bar{D}_1$
0	0	1	0	D_2	$\bar{D}_2$
0	0	1	1	D_3	$\bar{D}_3$
0	1	0	0	D_4	$\bar{D}_4$
0	1	0	1	D_5	$\bar{D}_5$
0	1	1	0	D_6	$\bar{D}_6$
0	1	1	1	D_7	$\bar{D}_7$



Pin Diagram

Saturday
04-03-17

16-to-1 (Multiplexer IC-74150)



Enable / Strobe ($\bar{E}$)	S_3	S_2	S_1	S_0	$Y = \bar{D_n}$
1	X	X	X	X	0
0	0	0	0	0	$\bar{D_0}$
0	0	0	0	1	D_1
0	0	0	1	0	D_2
0	0	0	1	1	D_3
0	0	1	0	0	D_4
0	0	1	0	1	D_5
0	0	1	1	0	D_6
0	0	1	1	1	D_7
0	1	0	0	0	D_8
0	1	0	0	1	D_9
0	1	0	1	0	D_{10}
0	1	0	1	1	D_{11}
0	1	1	0	0	D_{12}
0	1	1	0	1	D_{13}
0	1	1	1	0	D_{14}
0	1	1	1	1	D_{15}