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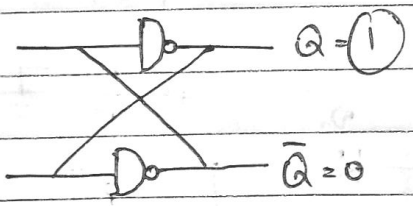
NOT Gate from NAND Gate

A	A	Y
0	0	1
1	0	-
0	1	-
1	1	0

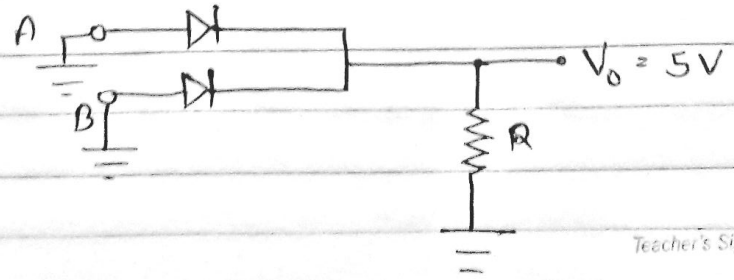
$Y = \overline{A \cdot A}$

$Y = \overline{A}$



1 bit data store Latch

Circuit diagram of OR gate by diode



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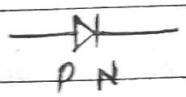
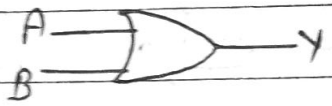
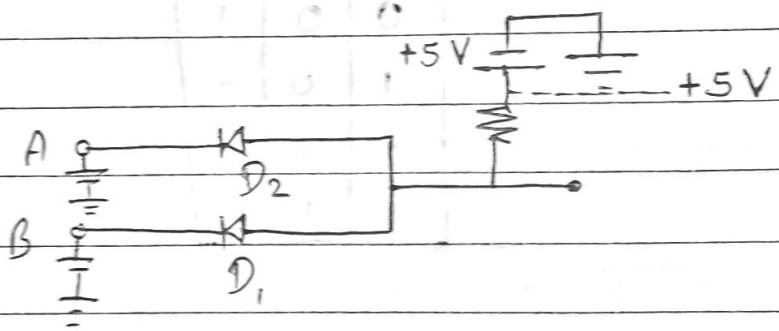
Digital Form

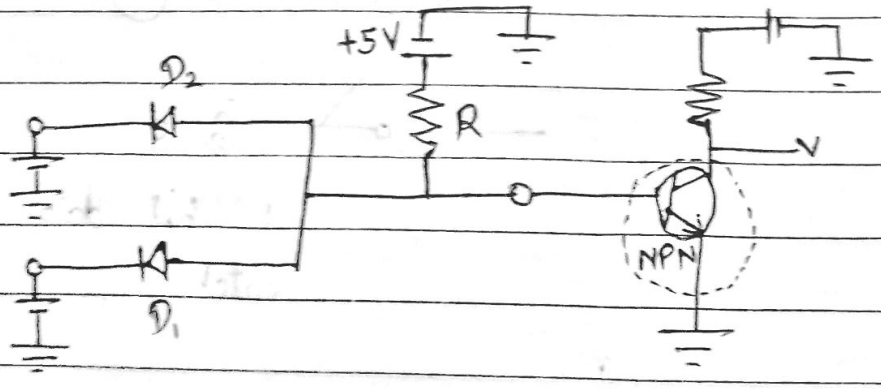




AND Gate using diode =>

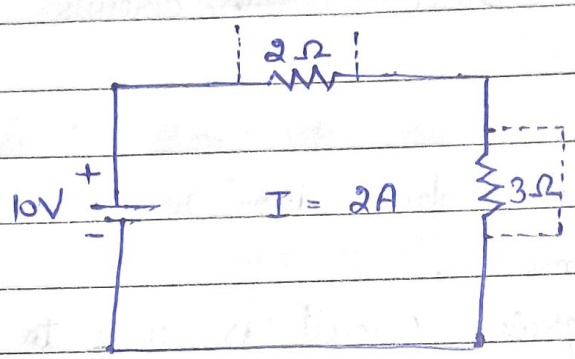


A = 0	B = 0	Y = 0
A = 1	B = 0	Y = 0
A = 0	B = 1	Y = 0
A = 1	B = 1	Y = 1



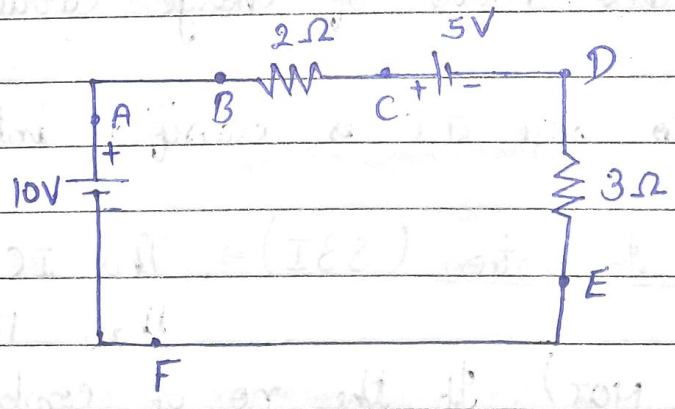
A	B	Y_1	Y
0	0	0	1
1	0	0	1
0	1	0	1
1	1	1	0

Referance →



$V_A = 10V$ $V_B = 0V$ $V_C = 0V$ $V_D = 0V$

$V_E = 0V$



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Integrated Circuit • (IC) ⇒ Electronic Circuit made by resistors, diodes and transistors which is used to realize logical expression, is called integrated circuit. It may contain multiple complicated circuit with large no. of components.

Example :- NAND & NOR ~~gates~~ circuits

This IC circuit contains two resistor, two diodes & one N-P-N transistor.

These integrated circuit is used to realize logical expression $\overline{A \cdot B}$.

IC is classified according to its size, nature of operation and nature of charge carrier.

According to size IC is classified into five types -

(1) Small Scale Integration (SSI) ⇒ This IC may contain less than 12 basic gates (AND, OR, NOT). If the no. of component (Resistor, Transistor, Diode) is less than 100 then it is small scale integration.

(2) Medium Scale Integration (MSI) ⇒ IC contain 12 to 99 basic gates to construct MSI. 100 to 999 basic components are used.

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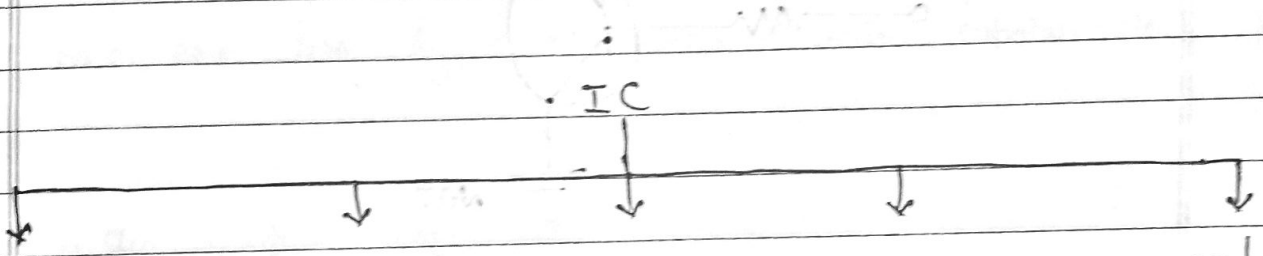
Large Scale Integration (LSI) ⇒ IC contain 100 to 999 basic gates to construct LSI & 1000 to 9999 basic components are used.

Very large Scale Integration (VLSI) ⇒ IC contain more than 1000 basic gates. To construct VLSI 10000 or more basic components are used.

Ultra Large Scale Integration OR Grand Scale Integration (ULSI/GSI)



	SSI	MSI	LSI	VLSI	ULSI / GSI
No of Basic gates	< 12	$12 \leq$ Basic Gates < 99	$100 \leq$ Basic gates < 999	$1000 \leq$ Gates	
No of Components	< 100	$100 \leq$ Components < 999	< 9999	$10000 \leq$ Component	

According to nature of operation IC is classified into two types -

1. Saturated Operation IC
2. Non-Saturated Operation IC

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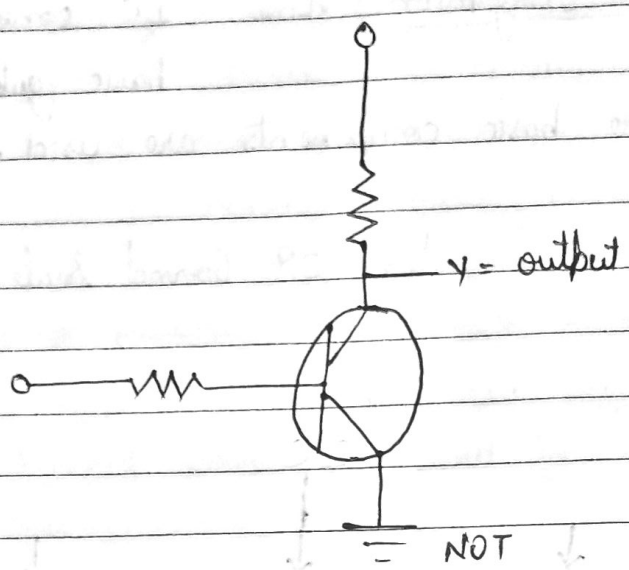
(1) Saturated Operation IC ⇒ In saturated logic families following circuits are used

(i) Resistor Transistor Logic (RTL) ⇒



(ii) Direct Coupled Transistor Logic (DCTL) ⇒ In this circuit transistor is coupled with resistor.

(iii) Integrated Injection Logic (I^2L) ⇒ It is made of transistor and diode.

(iv) Diode Transistor Logic (DTL) ⇒ It is designed by using diode and transistor.

(v) High Threshold Logic (HTL) ⇒ This logic family is operated at threshold ( ) voltage

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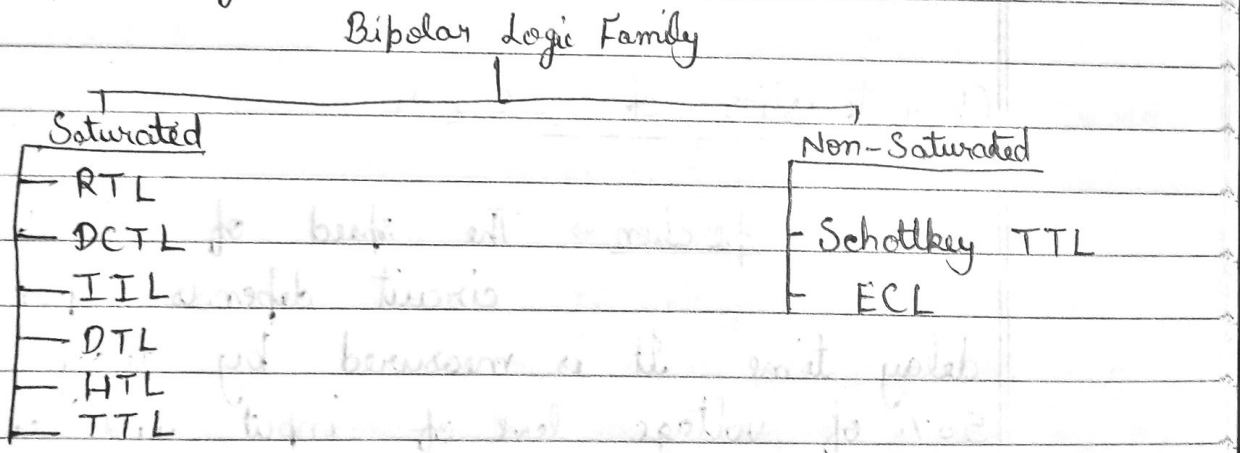
(vii) Transistor - Transistor logic (TTL) ⇒ All above logic family are operated on the saturation mode of diode & transistor.

(2) Non - saturated bipolar logic family ⇒ In bipolar family charge carrier will be electron & hole but in unipolar charge carries will be & electron only.

There are two types of Non - saturated bipolar logic families-

(i) Schottky TTL
(ii) Emitter Coupled Logic (ECL)



Unipolar Logic Family ⇒ There are three types of unipolar logic family. These devices are formed by metal oxide semiconductor field effect transistor (MOSFET). It is also known as MOS device.

There are three types of MOS device.

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MOS Device

PMOS — NMOS — CMOS

PMOS ⇒ P - channel MOSFET is called PMOS. In this device P - channel is employed.

NMOS ⇒ It is N - channel MOSFET. It is employed by N - channel of device.

CMOS ⇒ This device is known as complimentry MOSFET. This device is employed by P - channel & N - channel both.

Characteristics of IC's ⇒

Speed of Operation ⇒ The speed of operation of a digital circuit depends upon propagation delay time. It is measured by delay time between 50% of voltage leve of input and output waveforms.

Diagram

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Power Dissipation ⇒ The amount of energe disipate by IC per unit time is called power dissipation of IC's.

$$P_{diss} = I_{cc} V_{cc}$$

I_{cc} is the current through I_c and V_{cc} is the supplied potential difference to I_c. Its order will be milliwatt

$$1\ mW = 10^{-3}\ W$$

Figure of Merit ⇒ Figure of merit of depends upon propagation delay time & power disipation by IC. It is the product of propagation delay time and power.

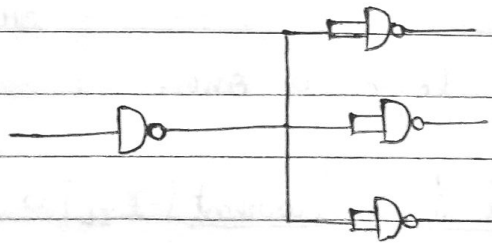
Figure of Merit = Propagation delay time × Power

$= (ns) \times (mW) = 10^{-9}\ s \times 10^{-3}\ W$

$= 10^{-12}\ Ws$

$=$ pJ (Picojule)

Fan Out ⇒ The no. of similar gates which can be driven by a single gate is called fan out.



This figure has fan out = 3

IC should have high fan out so that it operates more gates.

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Current and Voltage Parameter ⇒ For IC following current and voltage parameter are used.

(i) **High level input voltage** (V_{IH}) ⇒ This is the minimum input voltage which is recognise by gate when logic is one.

(ii) **Low level input voltage** (V_{IL}) ⇒ This is the maximum input voltage which is recognise by logic gate when logic is zero.

(iii) **High Level Output Voltage** (V_{OH}) ⇒ This is minimum output voltage which is recognise by gate when logic is ~~zero~~ one.

(iv) **Low Level Output Voltage** (V_{OL}) ⇒ This is maximum output voltage which is recognise by gate when logic is zero.

(v) **High Level Input Current** (I_{IH}) ⇒ This is the minimum input current which is recognise by gate when logic is one.

(vi) **Low Level Input Current** (I_{IL}) ⇒ This is the maximum input current which is recognise by the gate when logic is zero.

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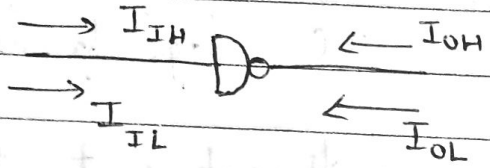
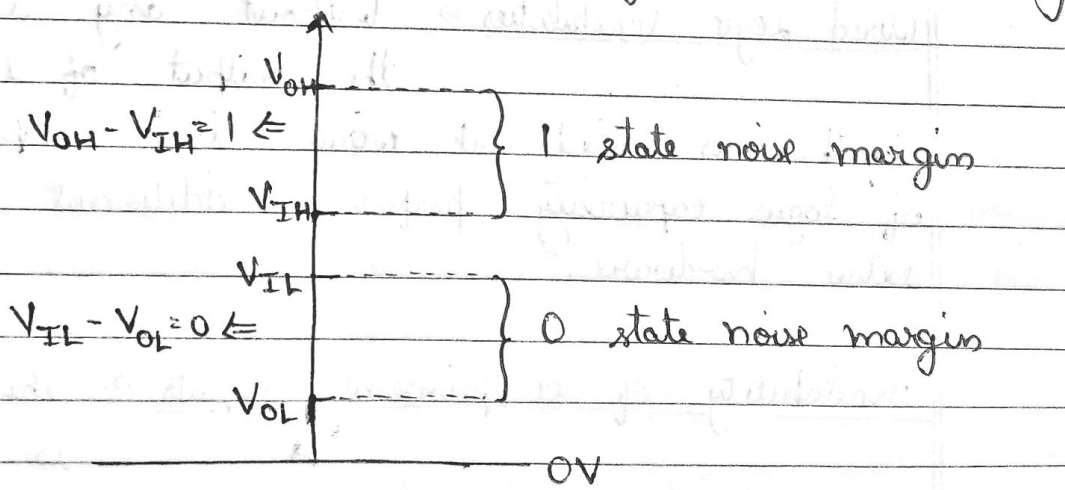
(vii) High Level Output Current (I_{OH}) ⇒ This is the minimum output current which is recognized by the gate when logic is one.

(viii) Low Level Output Current (I_{OL}) ⇒ This is the maximum output current which is recognized by the gate when logic is zero.



Noise Immunity ⇒ Stray electric and magnetic field may induce unwanted voltages to IC's that is called noise.

The ability of IC to tolerate noise is called noise immunity. IC should have high noise immunity



Power Supply Requirement ⇒ Amount of power or supplied voltage which is required by IC's to operate is called power supply requirement.

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Operating Temperature ⇒ The temperature range for which IC's function properly is known as operating temperature. Generally the range of operating temperature is 0°C to 70°C for user & industrial use and range of application for for military application will be -55°C to 125°C.

Flexibility Available ⇒ Various flexibilities are available for IC logic families.

(i) The breadth of series ⇒ It represent the type of different logic function available in series.

Popularity of series ⇒ It depends upon cost and other parameter per function. For this cost should be low.

Wired Logic Capabilities ⇒ Without any extra hardware the output of IC are connected together is called it wired logic capabilities. Such type of logic capability perform additional logic without any extra hardware.

Availability of compliment outputs ⇒ This property of IC is used to eliminate the need of additional inverters.

Type of Output ⇒ Passive pullup, Active pullup, open collector, drain, trasitate are known

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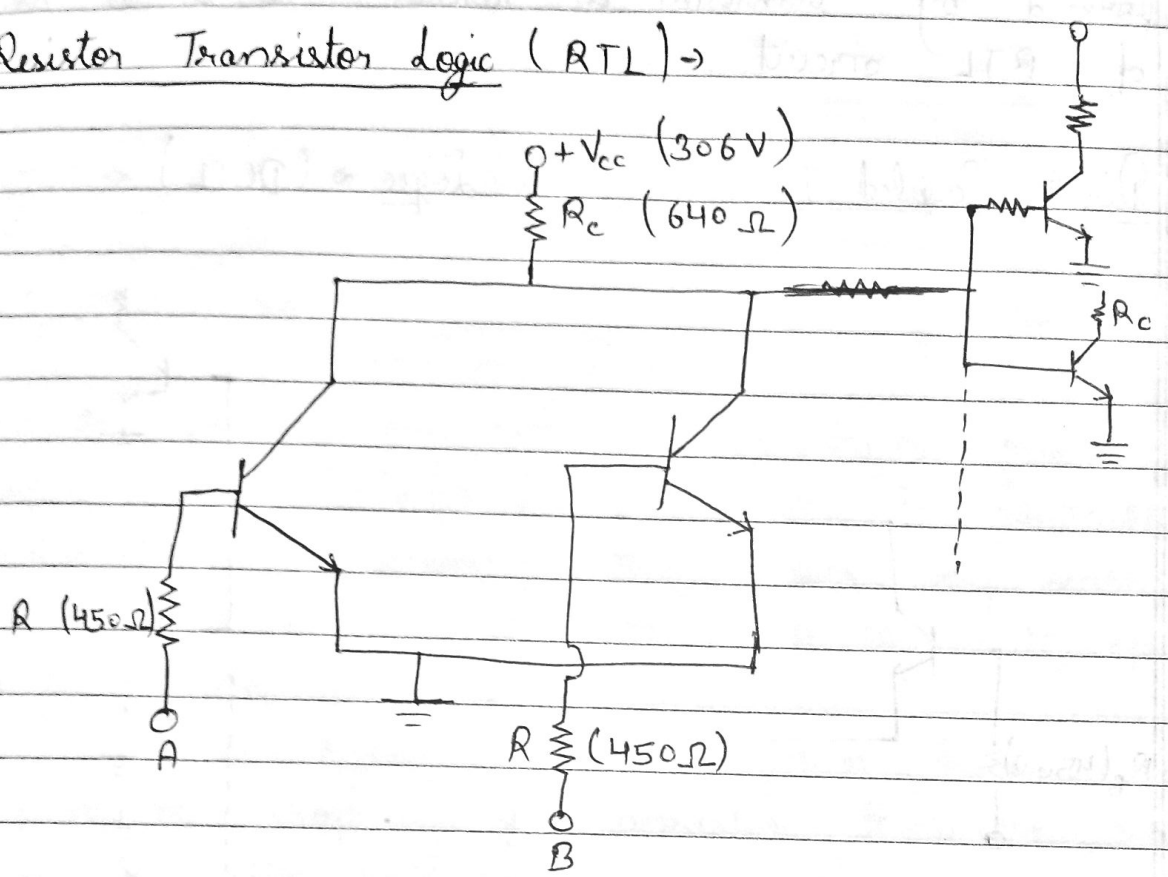
as type of output.

Resistor Transistor Logic (RTL) →



In given figure a resistor-transistor logic gate is shown. It is a basic RTL gate. It drives N load gates. Input circuit is behave like a NOR gate. So its fan in is N.

A	B	T_1	T_2	V_o (NOR)
0	0	OFF	OFF	1 (3.6V)
0	1	OFF	ON	0
1	0	ON	OFF	0
1	1	ON	ON	0

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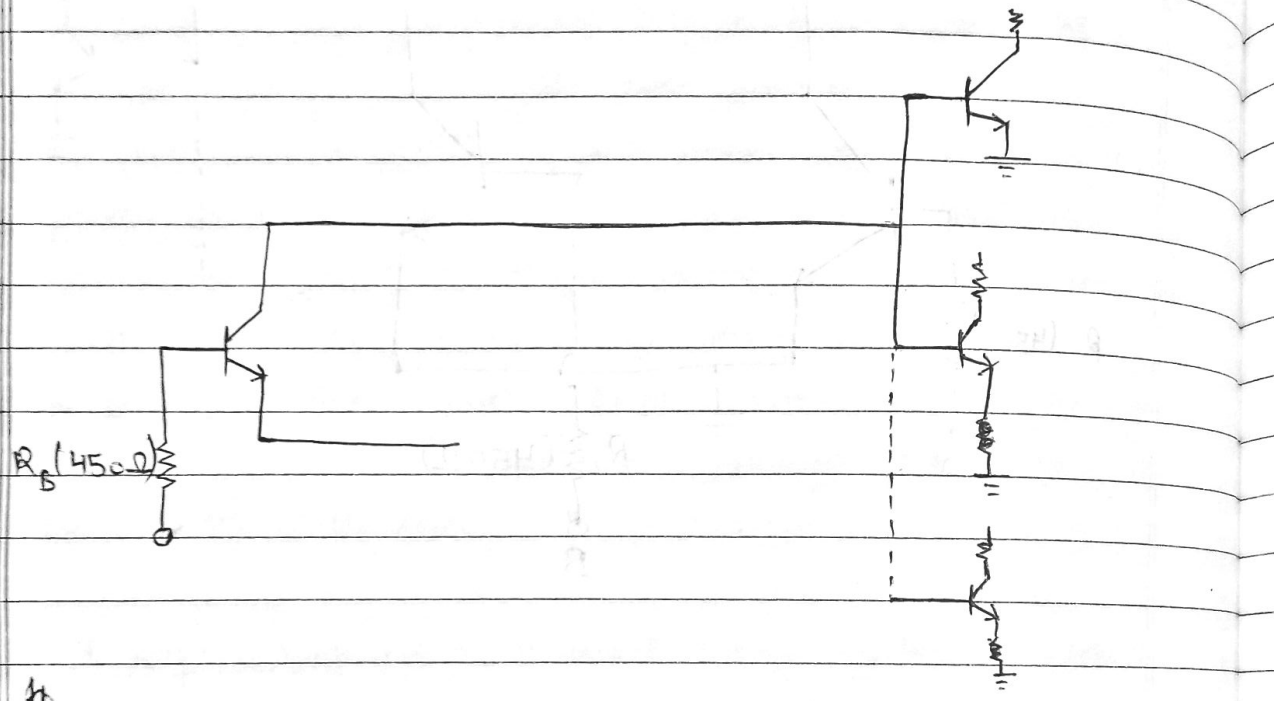
Input logic gate behave like a two input NOR gate. It is driving in similar gates as load. These gates are formed by transistor & resistor. So it is an example of RTL circuit.

Direct Coupled Transistor ~~Logic~~ Logic (DCTL) =>



If load gates are directly connected to outputs of input gates. Such circuits are called direct coupled transistor logic. It is similar to RTL but less useful due to current hogging.

The transistor with base emitter voltage ($V_{BE} = 0.78V$) when it enters in saturation region. It will not allow other transistor to enter in saturation region. In this case, total current supplied from driver gate. This is called current hogging.

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Integrated Injection Logic (I^2L)

Integrated injection logic is the specialized form of direct coupled transistor logic. It is easier to fabricate with Bipolar Junction Transistor (BJT). It uses very small chip area & consume less power. so it is easier to operate it at low voltage.

In given figure integrated injection logic is based on inverter property of transistor. It is also refer as Merge - transistor logic (MTL).

	V_{in}	T_1	T_{OI}
(I)	High (1)	ON	0
(II)	Low (0)	OFF	1

If input voltage for transistor T_1 is high the basic current B_1 will have two component, one due to V_{in} & other due to i_1.

Transistor T_1 is on, so i will be zero due to short between collector & Emitter terminal is short circuited. so potential drop at output will be zero.

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V_{01}	T_2	V_{02}
(Low) 0	OFFF	1
(High) 1	ON	0

We V_{in} each 0 that is at low potential then transistor T_1 will be off and output V_{01} will be 1. When V_{01} is 1 that is at high voltage, transistor T_2 is on & V_{02} will be zero.

When V_{01} is 0 that is at low voltage, transistor T_2 is off & V_{02} will be one.

So this circuit swings between 0 & 1 depends upon input voltage of transistor T_1.

Diode Transistor Logic (DTL)

This is 3 input (A, B & C) diode transistor logic (DTL). This current is driven by NAND gate. Load gates are similar to the driver gate.

The input diode D_A, D_B & D_C conduct & through resistance R. If corresponding input is low that

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output will be high, which is " input of transistor T so transistor T will be on, then output of transistor Y will be zero. then there will be no potential drop for load gates.

If input of diode D_A, D_B & D_C conduite through resistance R if corresponding input is high then output will be low that is 0 ! So transistor T will be off then output of transistor Y will be high or one. Then load gates are operated by NAND gate.

High Threshold Logic (HTL). Due to presence of electric motor on off ~~on~~ of control system high voltage ~~suddt~~ switches the noise level is ~~quiet his go~~ quite high. In this situation DTL circuit is redesigned which a high supply voltage (upto 15 volts) diode is replaced by zener diode & resistance is modified by its high value.

Such modifiers circuit is known as high ~~thre~~ threshold logic (HTL).

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A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

In this circuit driver gate behave like a NAND gate. It has three input the high thresold logic.

Load gate are operated by this drivers NAND gate.

The propagation delay is affected due to a large value of resistance R_1, R_2, R_C etc.

Due to zener diode potential difference at T_2 always regulate for the value of V_2.

HTL is less sensitive for temperature ~~then~~ than DTL circuit.

Transistor - Transistor Logic (TTL).

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DTL circuits has a speed limitation so it is outdated & replaced by transistor transistor logic.

TTL has operation speed faster than DTL but it work as DTL to that is diode is replaced by transistor.

Here driver gate behave like a three input TTL NAND gate.

Emitter Coupled Logic (ECL) ⇒ An emitter coupled logic (ECL) is the fastest logic gate in all logic families. So it is used in very high speed devices. The transistor which is used in ECL has different amplification configuration that configuration never drive in saturation mode.

Basic ECL circuits performing configuration has three input or has more that than three two gate different output.

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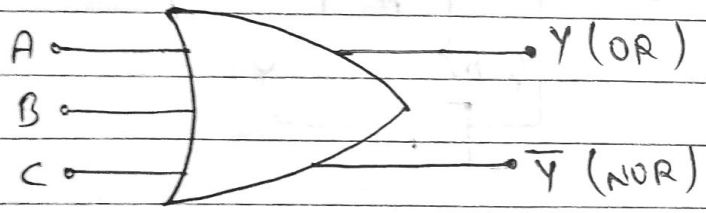
In given circuit three inputs A, B & C is given to base of transistor t_1' & t_1'' and t_1, the collector terminal of input transistor are connected to V_{cc} (high voltage)

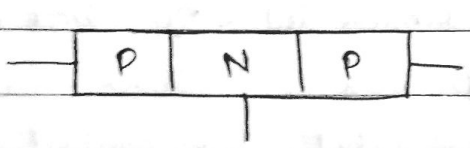
Emitter terminal input transistor are connect to $-V_{EE}$ (low voltage)

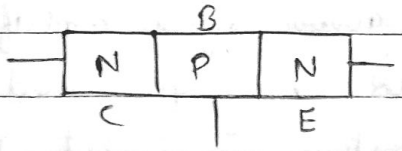
Differential amplifier is made of transistor t_1 & t_2 the inputs for differential amplifier is V_{i1} & V_{i2} output of differential amplifier is V_{01} & V_{02} these outputs are connected with T_3 and T_4 transistor. It works like input for transistor T_3 & T_4. Combination of transistor T_3 & T_4 known as emitter followers.

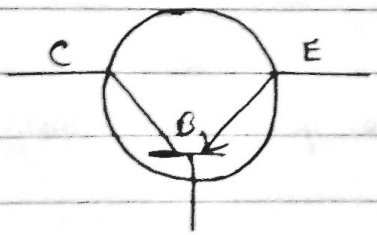
It emitter voltage gives output y_1 & y_2

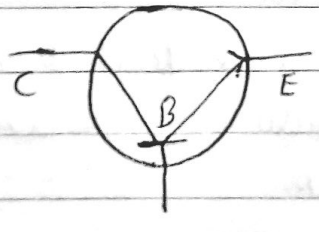


simplified circuit of given figure









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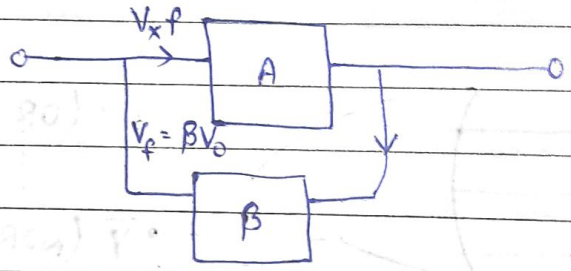
Feed Back Amplifier => If a part of output energy of an electrical network is transfer to its input that process is called feedback & such amplifier are known as feedback amplifier.

There are two types of feedback –

Positive Feedback => If feedback signal given to an amplifier is in phase with input signal that increase the magnitude of input signal. That is called positive feedback.

Negative Feedback => If feedback signal is out of phase with input signals is called negative feedback this decrease gain of amplifier.



In given figure amplifier is represented by box A & feedback network is represented by β box. Feedback network β feed V_f voltage to input V_i. Then input for amplifier will be V_{if}

For ideal feedback network

(i) There should be no change in the gain of amplifier due to β network.

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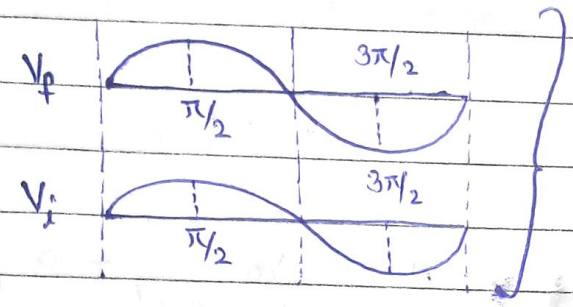
(ii) The input signal voltage must be transmitted by amplifier only.

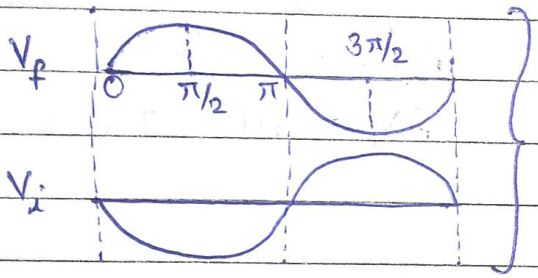
(iii) The feedback voltage must be transmitted through β network only.

(iv) Due to β network there should not be any loading on amplifier network / circuit.



in phase

phase difference = 0



out of phase

The resultant voltage at input after feedback is

$$V_{if} = V_i - V_f \quad \text{—①}$$

(for negative feedback)

$$V_{if} = V_i + V_f \quad \text{—②}$$

(for positive feedback)

from eq$_n$ → ① & ② for negative feedback

$$V_{if} = V_i - \beta V_o \quad \text{—③} \quad \text{(negative)}$$

$$V_{if} = V_i + \beta V_o \quad \text{—④} \quad \text{(for +ve)}$$

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Gain of amplifier is

$$A = \frac{\text{Output Voltage}}{\text{Input Voltage}} \quad \text{---(5)}$$

After feedback gain →

$$A = \frac{V_o'}{V_{if}} \quad \text{---(6)}$$

$$A = \frac{V_o'}{V_i - \beta V_o'} \longrightarrow \text{negative feedback}$$

$$A = \frac{V_o'}{V_i + \beta V_o'} \longrightarrow \text{positive feedback}$$

$$A(V_i + \beta V_o) = V_o'$$

$$AV_i = A\beta V_o' + V_o'$$

For negative feedback

$$V_o' = \frac{AV_i}{1 + A\beta}$$

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Let us consider

$$\frac{V_o'}{V_i} = A_f$$

Here $A\beta$ is known as loop gain of circuit for +ve feedback loop gain is ~~negative~~ positive & for negative feedback loop gain is +ve.

$1 - A\beta$ is known as return difference, it may be positive, negative or zero.

Case → I ⇒ If return difference is greater than one then A_f is less than A. This is the case for negative feedback.

$$|1 - A\beta| > 1$$

Case → II ⇒ If return difference is less than one then A_f is

Case → III ⇒ If return difference is 0 then A_f is infinity that is output voltage can be obtain without any input voltage. This is the condition for an oscillator.

Gain of amplifier with feedback also measured in decibal (dB). In dB formula for gain will be -

$$20 \log_{10}\left(\frac{A}{A_f}\right) = (20 \log_{10})(1 - A\beta)$$

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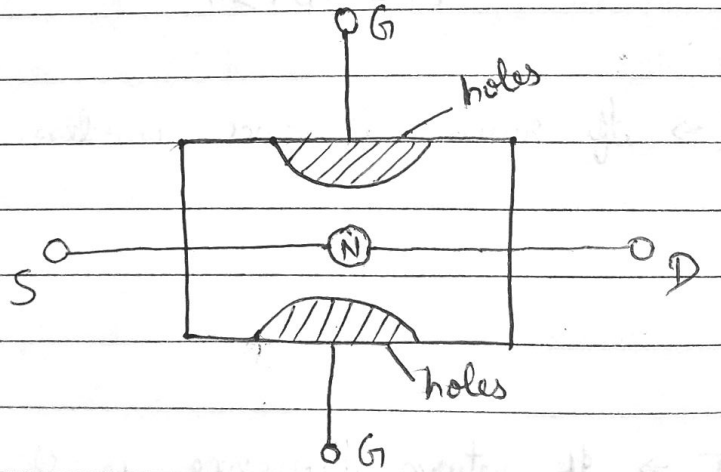
There are two type of FET
This is junction Field Effect Transistor (JFET)
MOSFET Metal ~~Oxide~~ Oxide semiconductor Field Effect Transistor

J-FET => It is n-type of or p-type doped transistor.
n-type has majority carrier electron & p-type has majority carrier hole. n-type semiconductor also known as n-channel FET.
p-type semiconductor also known as p-channel FET

The terminals of FET also ~~known as~~ called source (S) and drain (D), through these ends majority carrier flows. Majority carrier enters from source & leave it from drain. Two opposite faces in particular direction perpendicular direction to source drain line are heavily doped with opposite kind of impurities & known as gate (G).



N-channel JFET

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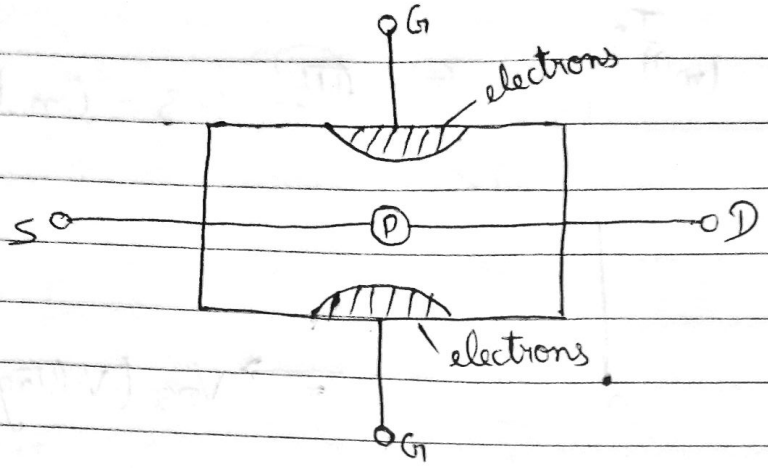


p - channel JFET

Electronic symbol for n & p channel JFET.

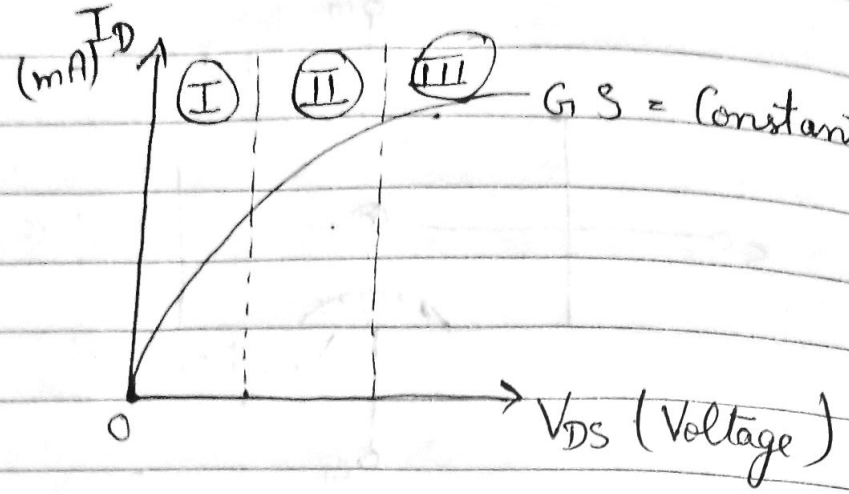
In source drain circuit of JFET the output or drain current I_D depends upon drain voltage & gate voltage.

V_{DS} ⟶ Drain Voltage

V_{GS} ⟶ Gate Voltage

If reverse bias voltage V_{GS} of gate remains constant then the family curves showing the dependence of drain current I_D with forward drain voltage (V_{DS}). This is known as common source drain characteristics.

Teacher's Signature.....



There are three region in characteristics curve

(i) <u>Resistive or Linear Region</u> => In this region I_D is proportional to V_{DS}

$$I_D \propto V_{DS}$$

(ii) <u>Saturation Region</u> => At the boundary of linear or Resistive region for V_{GS} = Constant, I_D remains constant that region is called saturation region. After that for constant value of I_D that is known as pinch of voltage region.