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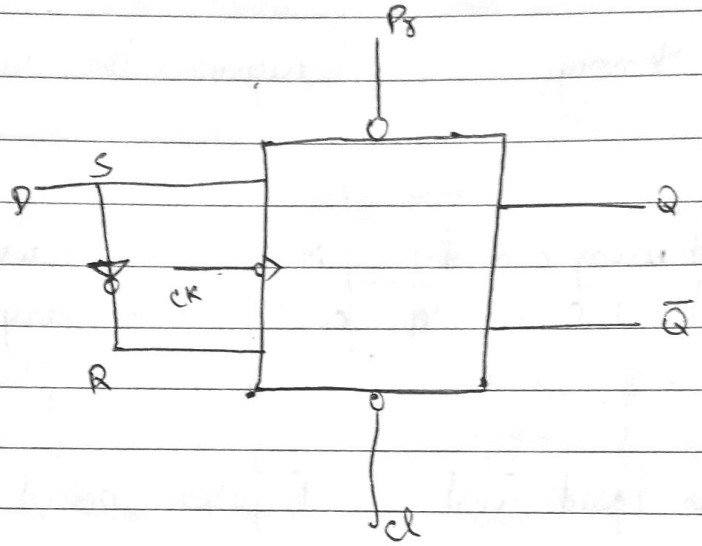
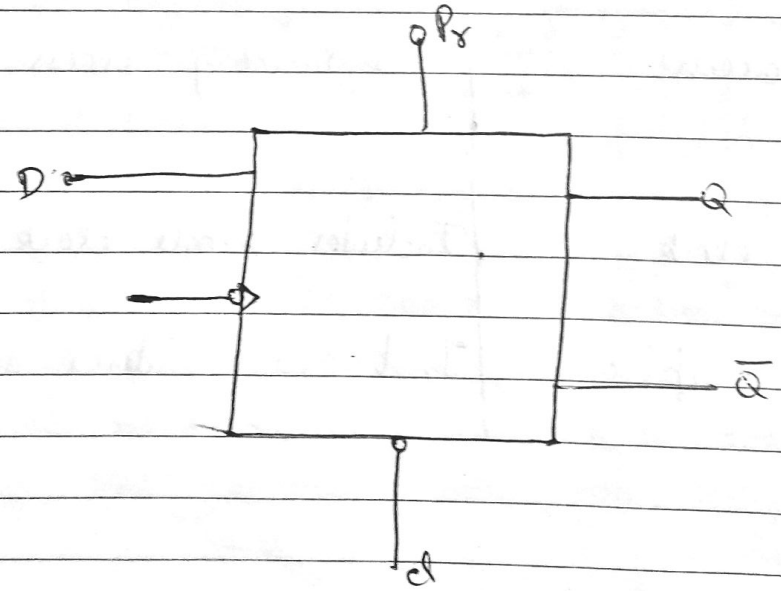
Physics

D Flip-Flop → If input of clocked R-S Flip flop is connected with each other with the help of NOT gate. The input for S & R will be "1, 0" or 01 that FF is called D FF. because the transfer of data from input to output is delayed.





TRUTH TABLE

D	Q_{n+1}	$\bar{Q}_{n+1}$
0	0	1
1	1	0

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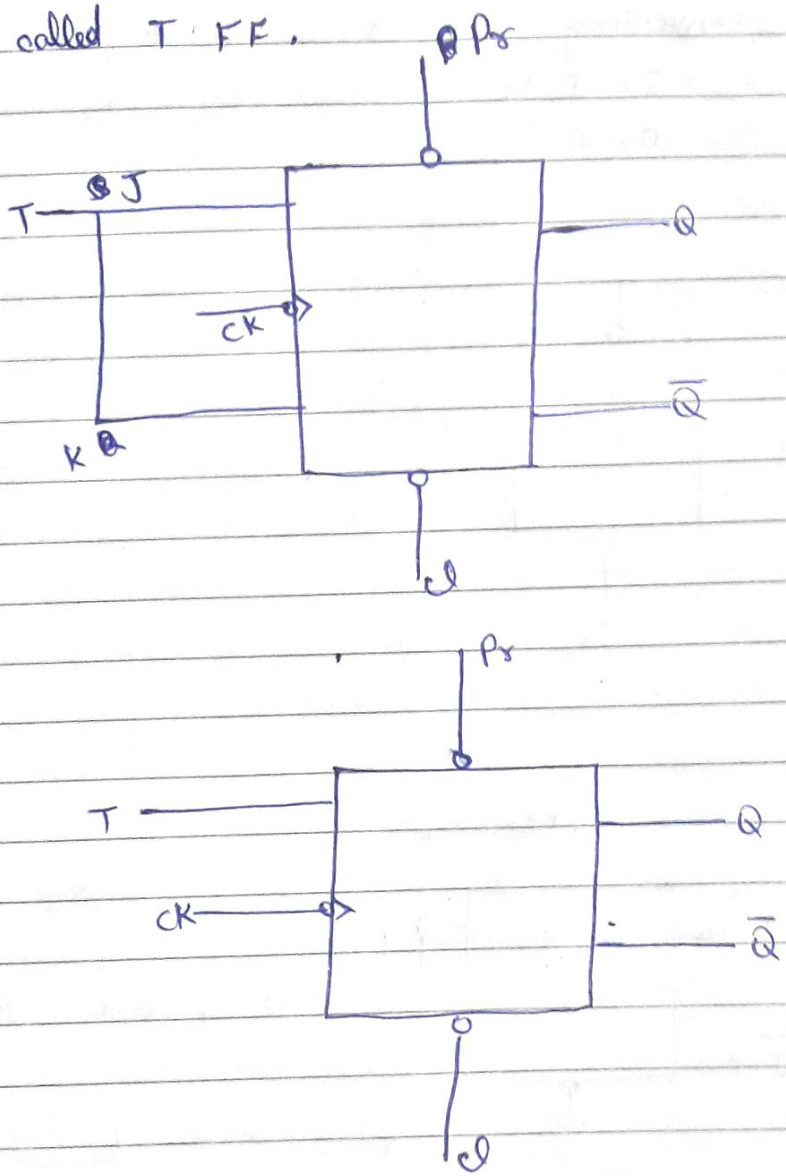
T Flip Flop → When inputs J-K f.f connected with each other it behave like a toggle switch, so it is called T FF.



Truth Table

T	Q_{n+1}	$\overline{Q}_{n+1}$
0	Q_n	$\overline{Q}_n$
1	$\overline{Q}_n$	Q_n

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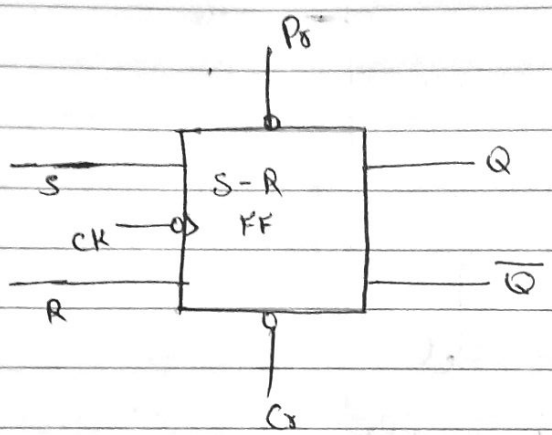
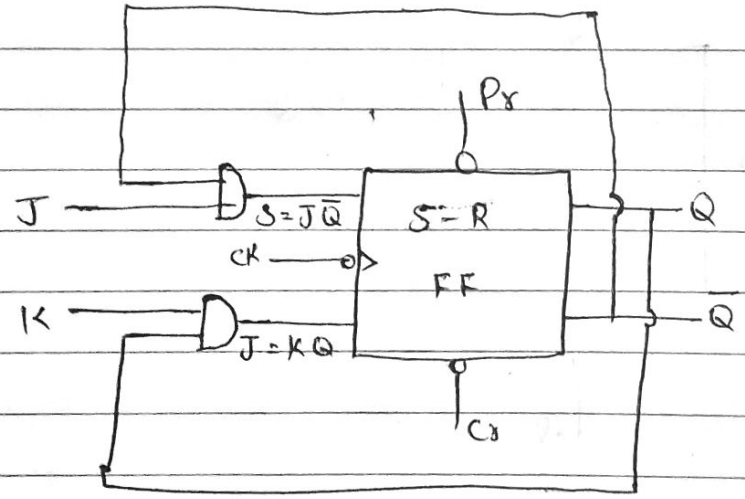
J-K Flip Flop → The uncertainity in the state of S-R flip flop i.e. S = R = 1 can be eleminated by converting into a J-K f.f.

$$S = J \cdot \overline{Q}$$

$$R = K \cdot Q$$





X

J	K	S	R	Q_{n+1}	$\overline{Q}_{n+1}$
0	0	0	0	Q_n	$\overline{Q}_n$
1	0			1	0
0	1			0	1
1	1			$\overline{Q}_n$	Q_n

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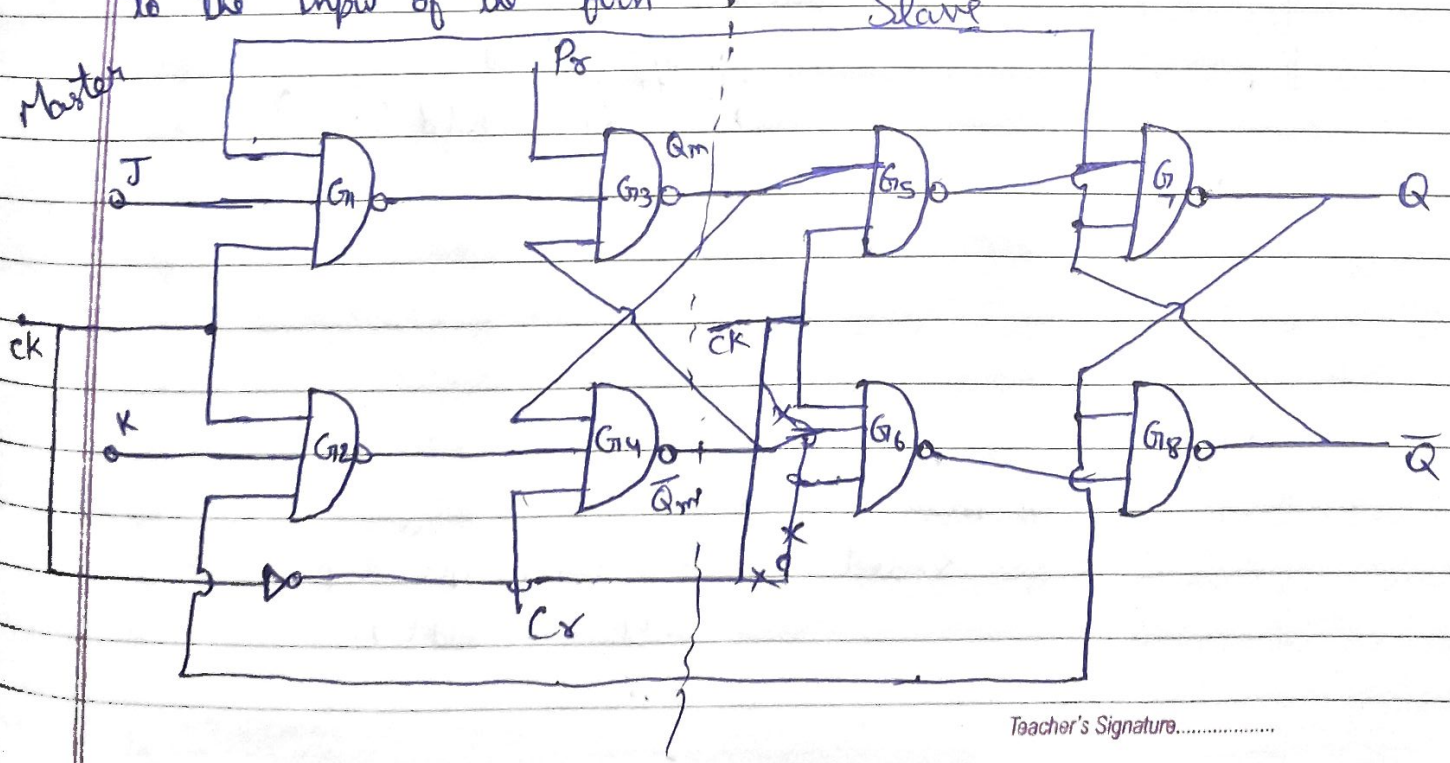
J_n	K_n	Q_n	$\bar{Q}_n$	S_n	R_n	Q_{n+1}	$\bar{Q}_{n+1}$
0	0	0	1	0	0	$Q_n = 0$	$\bar{Q}_n$
0	0	1	0	0	0	$Q_n = 1$	$\bar{Q}_n$
1	0	0	1	1	0	1	0
1	0	1	0	0	0		
0	1	0	1	0	0	0	1
0	1	1	0	0	1	0	1
1	1	0	1	1	0	$\bar{Q}_n$	Q_n
1	1	1	0	0	1	$\bar{Q}_n$	Q_n

Master slave J-K flip flop → It is a cascade of two S-R ff with feedback forom the outputs of the second to the input of the first.



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Physics

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Master slave J-K f·f

Gate G_1, G_2, G_3 & G_4 form Master flip-flop the clock for Master flip-flop will be positive or positive edge triggered Master flip-flop is same as J-K flip-flop. Output will be Q_m & $\bar{Q}_m$. When ck = 1 master flip-flop is enabled & gives output Q_m & $\bar{Q}_m$.

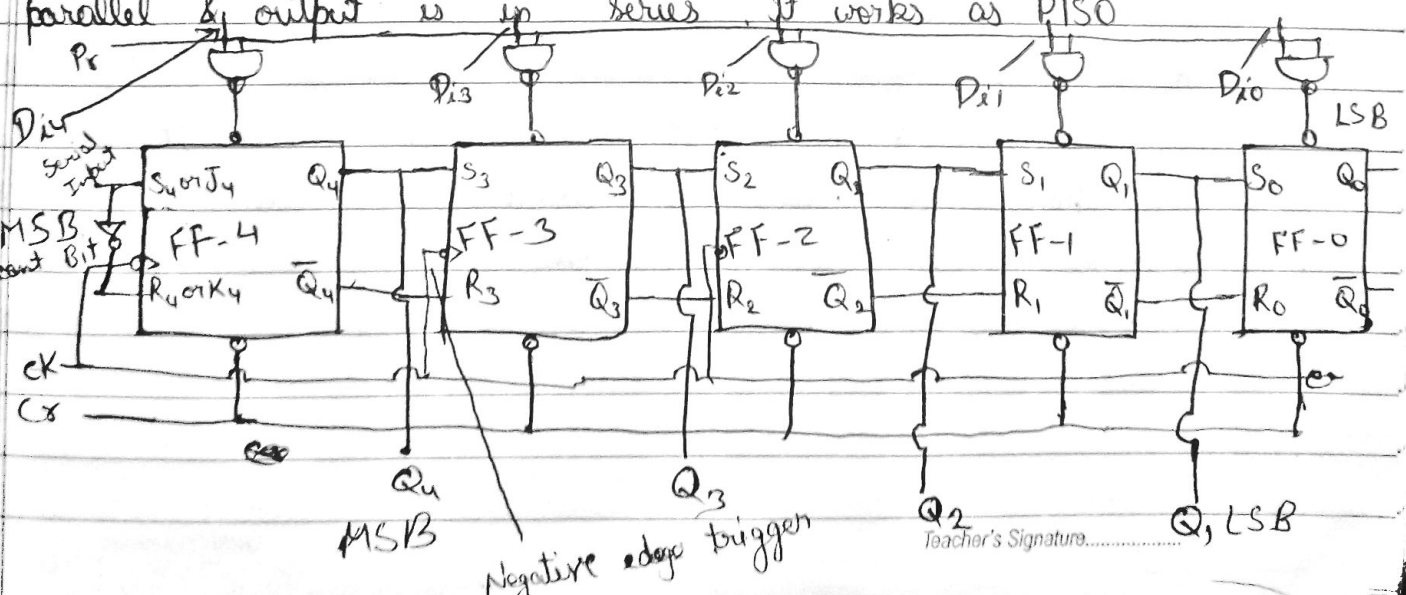
G_5, G_6, G_7 & G_8 form slave flip-flop. When ck is 1 then clock for slave flip-flop $\bar{ck} = 0$. This time slave flip flop is disabled.

When ck = 0 master flip-flop is disabled and slave f·f is enabled. Slave flip-flop gives output after a pulse delay where master ff is operated. The input of slave f·f commanded by output of master f·f. The final output depends upon clock pulse given to Master flip flop. Truth Table for Master & Slave f·f will be same as J-K f·f.

Master slave f·f is designed to overcome race around difficulty, so that the uncertainity in output of J-K flip-flop is removed.

IC-7496

Shift Register → A five bit shift register is made of Master Slave f·f. For this shift register inputs are parallel & output is in series. It works as PISO



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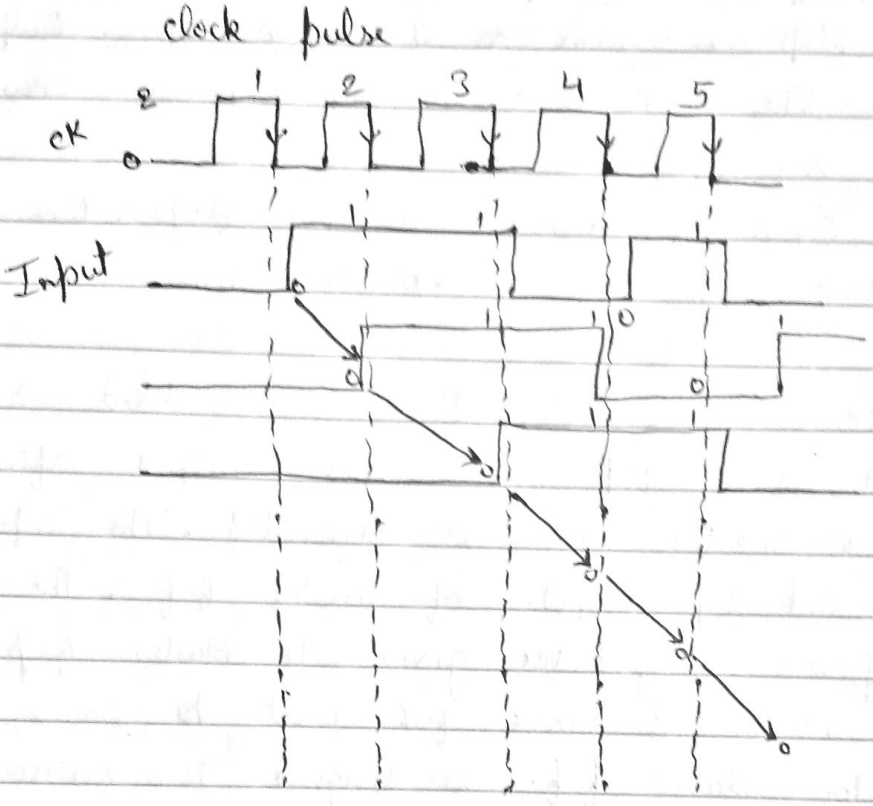
→ Negative edge triggered → Positive edge triggered

Waveform of shift register for serial input →



Ripple

Synchronous ~~Counter~~ & Asynchronous Counter → If all flip-flops in a counter are not clocked simultaneously that counter is called ripple counter.

If all flip-flops are clocked simultaneously that counter is called synchronous counter.

A circuit used for counting the pulse is known as counter.

If the no of state in counter is N. It is known as Modulo N counter & divide by N counter, for ring counter N state is known as module N but other counter known as 2N Modulo counter.

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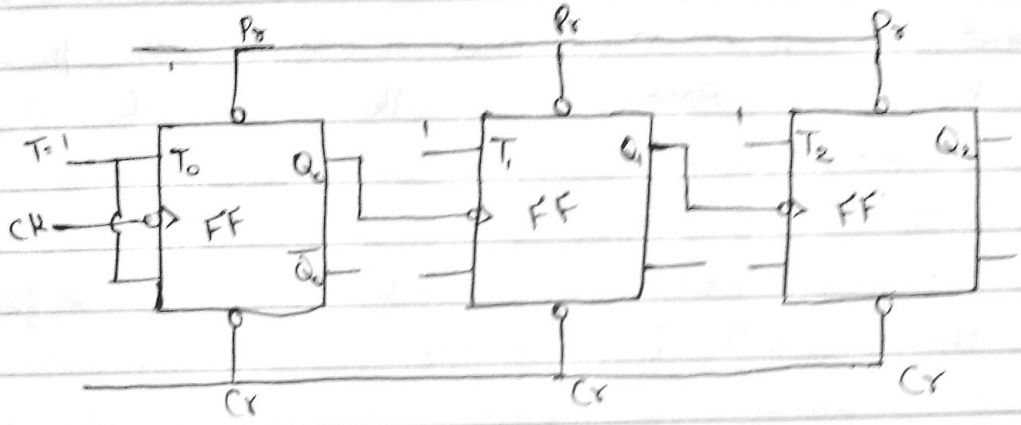
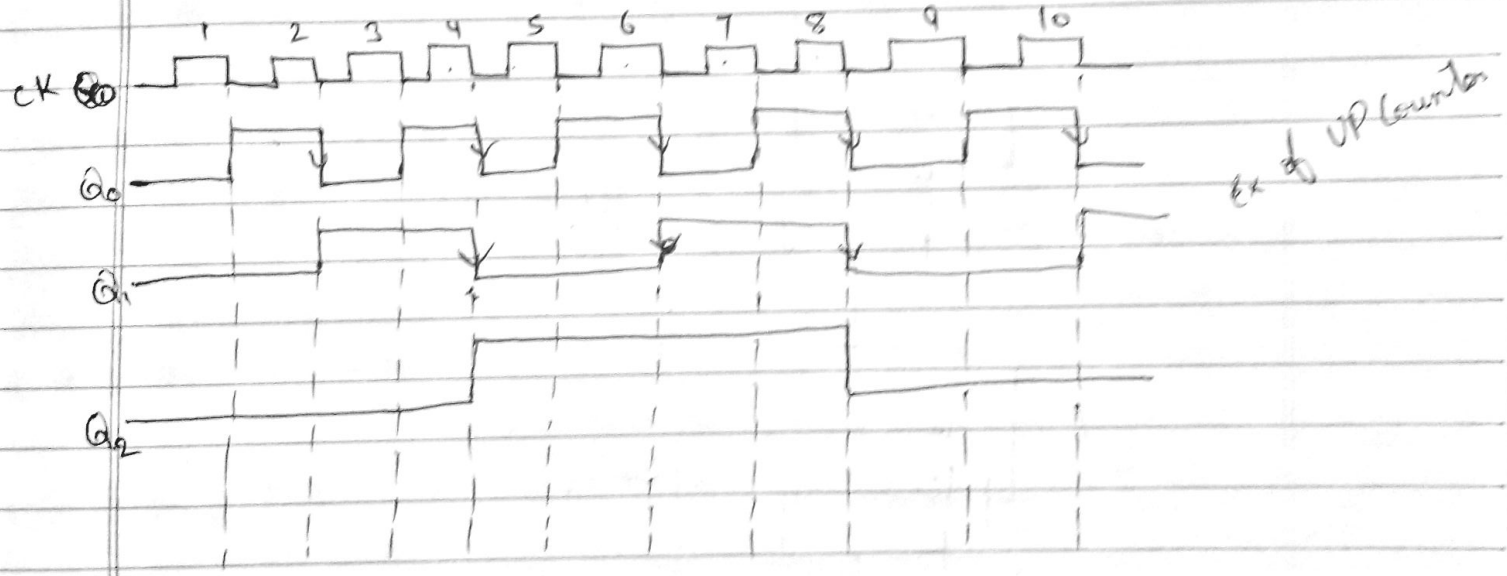
A 3-bit binary counter →





Ex of UP counter

UP & DOWN Counter → If the output of counter increases with successive clock pulse. It is called UP counter. It is triggerd with negative edge clock.

If the output of counter decreases with successive clock pulse. It is called DOWN counter. It is triggered with positive edge clock.

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input H=0, L=1] Negative Logic
input H=1, L=0] Positive Logic

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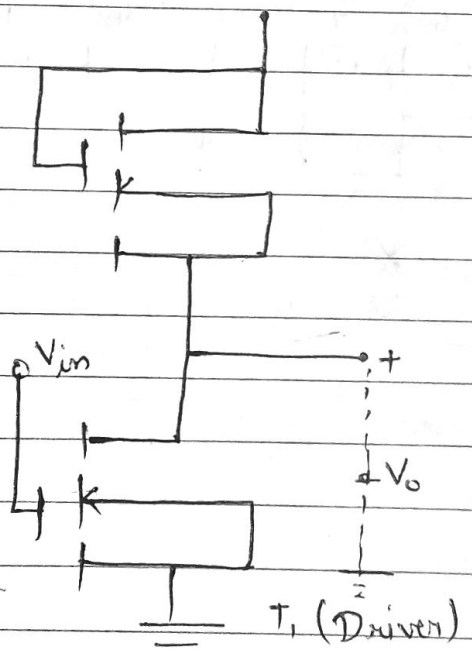
MOSFET => (Metal Oxide Semiconductor Field Effect Transistor) => MOSFET circuit is used due to high density of fabrication & low power dissipation. When MOSFET is used in devices circuit has p or n channel ⊛ circuit with p channel is known as PMOS. © & with n channel is known as ⊛ NMOS

Charge carrier for p channel will be hole & for N. channel will be electron

MOSFET inverter



Most logic is used for design of LSI & VLSI IC's. It is not used for SSI & MSI. Most of the microprocessor memories & peripheral devices formed by MOSFET circuit.

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