BCA Second Semester Examination- May 2015

THIRD PAPER

Digital Electronics & Circuits

Paper Code : 2731

me Allowed: Three Hours **Maximum Marks-70**

(1) No supplementary answer book will be given to any candidate. Hence the candidates should write the answers precisely in the main answer book only.

(2) All the parts of one question should be answered at one place in the answer book. One complete question should not be answered at different places in the answer book.

(Attempt all six questions.)

Part I (Question No. 1& 2) is compulsory & part II (Question No. 3, 4 , 5 & 6) has internal choice.

PART-I

Answer any 10 questions out of the following. Each question carries 1 mark. **10x1= 10**

a) What is standard and SOP form ?

b) What are Universal Logic Gates ?

c) What is Ex-NOR gate ?

d) What do you mean by don't care state ?

e) What is DCTL gate ?

f) What is the major advantage of CMOS gates ?

g) What do you mean by Sequential Circuits ?

h) What is a Priority Encoder ?

i) What is D Flip-Flop ?

j) What is the relation between Flip-Flop and Latch ?

k) What is Shift Register ?

l) What are the advantages of synchronous counter ?

. Answer all the questions. Each question carries 5 marks. **4x5= 20**

a) Explain the working of OR gate.

b) Discuss various logic families.

c) Explain the working of BCD to seven segment De-coder.

d) Explain the working of RS Flip-Flop.

P. T.O.

PART-II

Unit I

3. (a) Minimize the following logical function using K-map

$$f(A, B, C, D) = \sum m\,(1,5,6,12,13,14) + d(2,4)$$

(b) Realize the reduced expression using NAND gates.

OR

(a) Expand $A + B\overline{C} + AB\,\overline{D} + ABCD$ to minterms and maxterms. Express the above expression in standard SOP and standard POS form.

(b) Draw the Circuit diagrams for the synthesis of AND, OR and NOT gates using only NOR gates.

Unit II

4. (a) Draw and explain DCTL NOR gate.

(b) Compare TTL and CMOS with respect to fan in, fan out, noise margin, propagation delay, and power dissipation.

OR

(a) What are different characteristics and comparison of the major logic families ?

(b) Write the difference between positive and negative logic.

Unit III

5. (a) Explain the working of Decimal to BCD priority encoder.

(b) Explain the working of 8 : 1 mutiplexer.

OR

(a) Explain the construction and working of 1 : 16 Demultiplier.

(b) Explain the working of parity checker and draw the pin-out diagram for IC 74180 parity checker.

Unit IV

6. (a) What do you mean by race around condition in J-K flip-flop ? How it can be avoided ? Explain.

(b) Explain the construction and working of Master-Slave flip-flop.

OR

(a) Draw the four stages of shift left, shift right register and explain its working.

(b) Differentiate between Synchronous and Asynchronous Sequential Counters.

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