BCA Second Semester Examination May-2016

THIRD PAPER

Digital Electronics & Circuits

Paper Code:- 2731

Time Allowed: Three Hours **Maximum Marks.70**

(1) No supplementary answer book will be given to any candidate. Hence the candidates should write the answers precisely in the main answer book only.

(2)All the parts of one question should be answered at one place in the answer book.

(Attempt all six questions.)

Part I (Question No. 1& 2) is compulsory & Part II (Question No. 3, 4 , 5 & 6) has internal choice.

Part-I

1. Answer any 10 questions. Each question carries 1 mark. **10x1= 10**

(Word limit up to 20 words each)

a) Write the truth table and symbol for XOR gate.

b) Explain miniterms and maxterms in digital Electronics.

c) What is Karnaugh Map ?

d) What do you understand by Field-effect Transistor ?

e) Draw the circuit for Diode Transistor Logic (DTL) NOR gate.

f) What is Race Around Condition ?

g) What is the difference between Multiplexer and Demultiplexer ?

h) Define Decoder and Encoder.

i) Explain T-type flip-flop.

j) What are combinational logic circuits ?

k) Define Sequential Logic circuits.

l) Write the drawback of J-K flip-flop.

2. Answer all the questions. Each question carries 5 marks. **4x5 = 20**

(Words limit up to 50 words each)

a) What are logic gates ? Obtain NOT, AND, OR gates with the help of NOR logic gate.

b) Explain the working of Resistance Transistor Logic (RTL) NOR gate.

c) Explain the modes of operation of Shift Register.

d) Explain the working of decimal to BCD priority Encoder.

P.T.O.

Part-II

Unit-I

3. (a) Plot the following Boolean function on a Karnaugh map and simplify it. 5

$F = m_8 + m_9 + m_{10} + m_{11} + m_{12} + m_{13} + m_{14} + m_{15}$

(b) Prove that all logic operations can be performed using NAND gates. 5

OR

(a) Simplify the following Boolean function in
(i) Sum of Products and (ii) Products of Sums $F(A,B,C,D) = \sum(0,1,2,5,8,9,10)$ 7

(b) Draw the logic diagram for the following expression. 3

$\overline{A+B} \oplus \overline{A}.\overline{B} = R$

Unit-II

4. (a) Explain how using P-N diodes and transistor the following gate operations can be obtained. 5
(i) AND (ii) OR (iii) NOT (iv) XOR

(b) Write the important characteristics of ECL devices. 5

OR

(a) Explain the I-V characteristic of a Junction Field Effect Transistor (JFET). 5

(b) Write the advantage of CMOS over the TTL at the following features 5
(i) Fan in (ii) Fan out (iii) Noise Margin (iv) Propagation delay (v) Power dissipation.

Unit-III

5. (a) Explain the construction and working of 16 : 1 multiplexer. 5

(b) Explain the working of BCD to seven segment Decoder driver. 5

OR

(a) Draw the pin-out diagram for IC 74180 parity checker and explain the working of it. 5

(b) Explain the construction and working of 1 : 16 Demultiplexer. 5

Unit-IV

6. (a) Explain the working of JK flip flop. Describe its merits over clocked R-S flip flop. 5

(b) Explain the construction and working of shift-right register using D-flip flop. 5

OR

(a) Explain the construction and working of UP/DOWN counter. 5

(b) Explain D-type flip flop. Show that a D-type flip flop can be converted to a JK flip flop. 5

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